

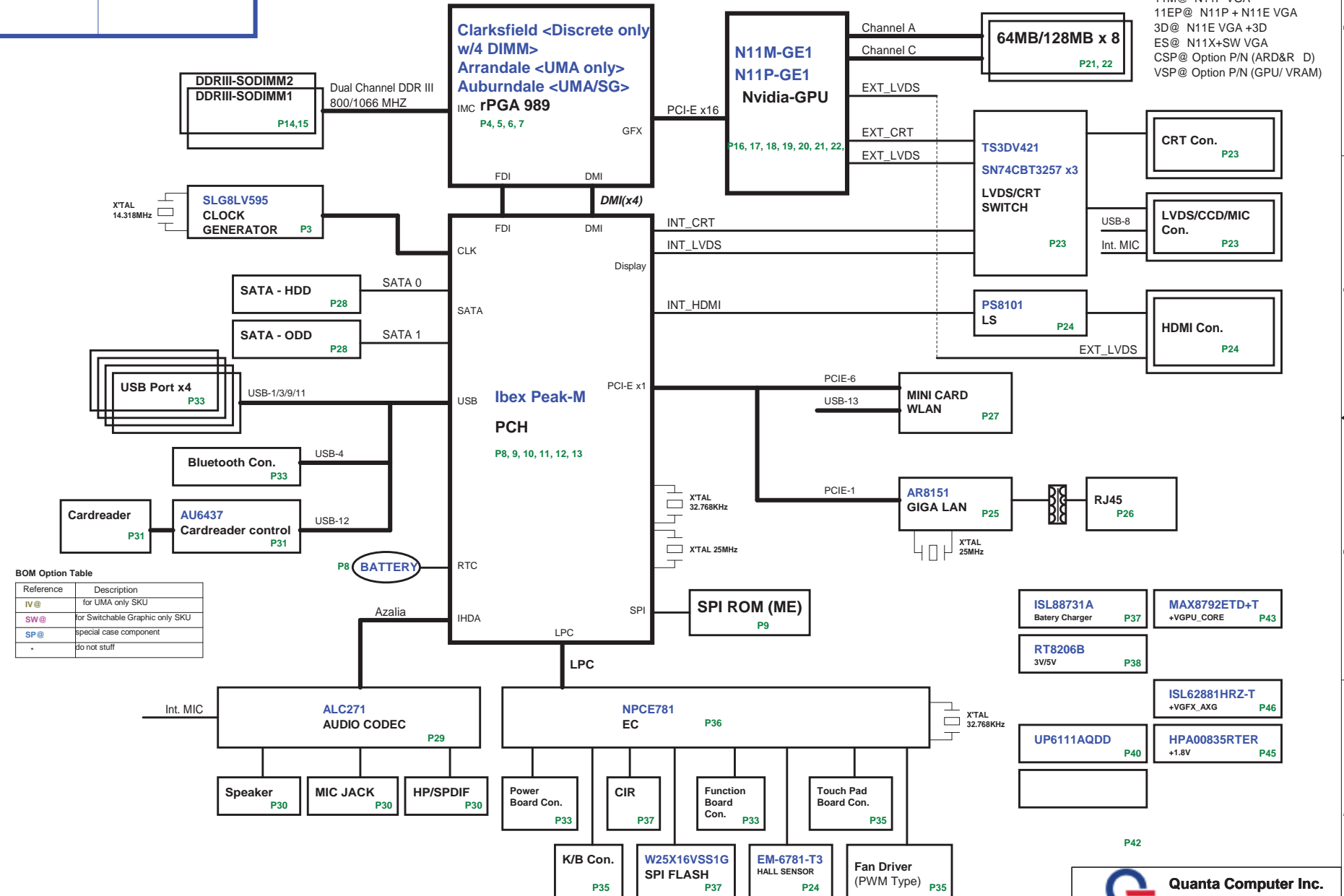
VER : 1A

BOM P/N Description

ZR7 SYSTEM BLOCK DIAGRAM

BOM MARK

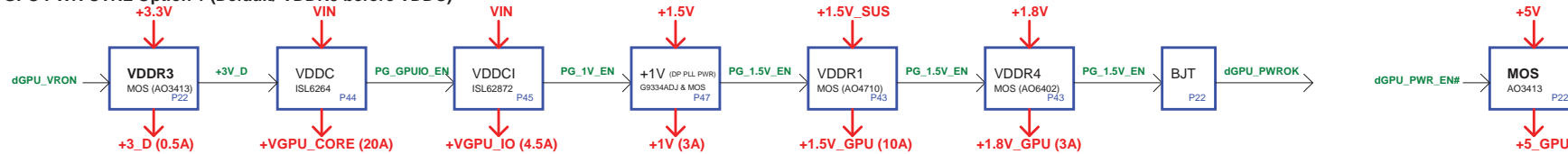
IV@ INT VGA
EV@ DISCRETE
SW@ SW VGA
11P@ N11P VGA
11M@ N11P VGA
11EP@ N11P + N11E VGA
3D@ N11E VGA +3D
ES@ N11X+SW VGA
CSP@ Option P/N (ARD&R D)
VSP@ Option P/N (GPU/ VRAM)



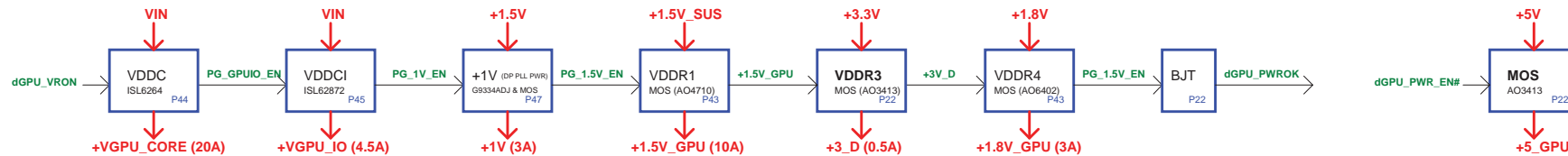
BOM Option Table

Reference	Description
IV@	for UMA only SKU
SW@	for Switchable Graphic only SKU
SP@	special case component
*	do not stuff

GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDC)



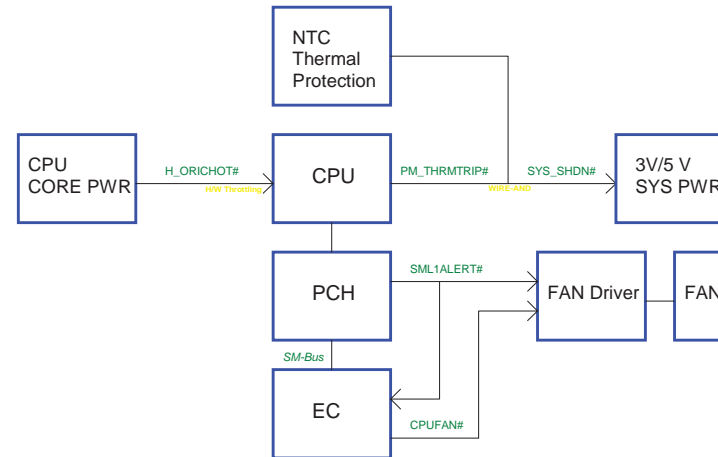
GPU PWR CTRL Option 2 (VDDR3 after VDDR1)



Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+VCCRTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BIOS/CI/ POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	GFX_ON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.1V_VTT	+1.05V or +1.1V	CPU VTT POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER	MAINON	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+5V_GPU	+5V	SWITCHABLE PWM IC POWER	dGPU_PWR_EN#	Discrete enable
+GPU_CORE	+0.9V~+1.1V	GPU CORE POWER	+3V_D	Discrete enable
+GPU_IO	+0.9V~+1.1V	GPU I/O POWER	PG_GPUIO_EN	Discrete enable
+1.5V_GPU	+1.5V	VRAM CORE POWER	PG_1.5V_EN	Discrete enable
+1.8V_GPU	+1.8V	GPU_CRE/LVDS/PLL POWER	+1.5V_GPU	Discrete enable
+1V	+1V	DP/PEG POWER	PG_1V_EN	Discrete enable

Thermal Follow Chart



ARRANDALE/CLARKSFIELD PROCESSOR (DDR3)

U37C

Clarksfield/Auburndale

DDR SYSTEM MEMORY A

Channel A DQ[11,15,19,32,35,42,46,48,54,60], DM[5]
Requires minimum 12mils spacing
with all other signals, including data signals.

U37D

Clarksfield/Auburndale

DDR SYSTEM MEMORY - B

Channel B DQ[11,16,18,19,36,42,51,55,56,57,60,61,62]
Requires minimum 12mils spacing
with all other signals, including data signals.



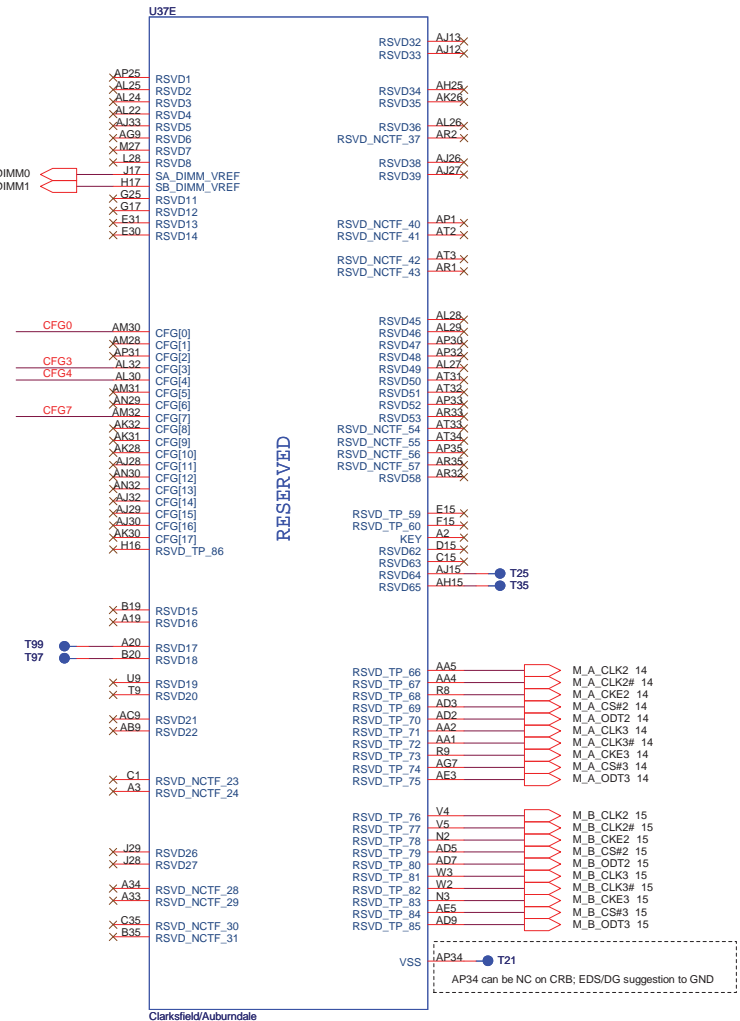
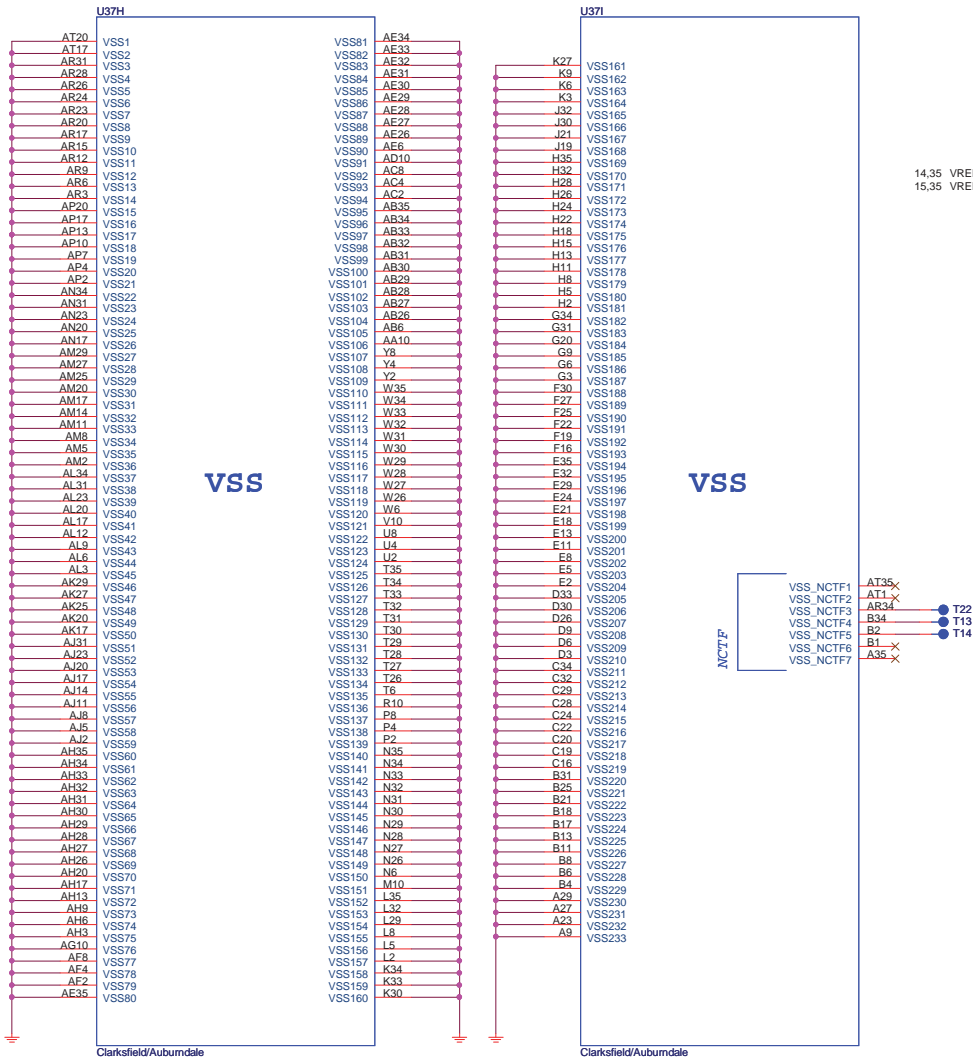
Quanta Computer Inc.
PROJECT : ZR7

Size	Document Number	Rev
	ARRANDALE/CLARKSFIELD 2/4	3B
Date:	Monday, February 22, 2010	Sheet 5 of 49



ARRANDALE/CLARKSFIELD PROCESSOR (GND)

ARRANDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)

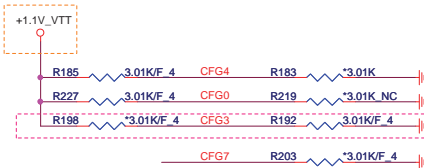


Processor Strapping

	1	0	DEFAULT
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled	1
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed	1
CFG4 (Embedded Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port	1
The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.			

VTT Rail Values are
Arrandale VTT=1.05V
Clarksville VTT=1.1V

Use reverse type



The schematic diagram illustrates the RTC module circuit. It features a +3VPCU input connected to a BAT54C diode (CR1) and a +VCCRTC input connected to a network of resistors (R678, R677, R674, R678) and capacitors (C768, C769, C784, C753). The RTC module (RT1) is connected to the VCCRTC_1 and VCCRTC_2 lines. The output of the RTC module is connected to the RTC_RST# pin, which is also connected to a network of resistors (R678, R674, R678) and capacitors (C768, C769, C784, C753). The circuit is powered by a +5V_SS supply.

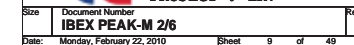
29 PCH_AZ_CODECS_SYNC R653 33.4 ACZ_SYNC

29 PCH_AZ_CODECS_RST# R659 33.4 ACZ_RST#

29 PCH_AZ_CODECS_SDOUT R658 33.4 ACZ_SDOUT

29 PCH_AZ_CODECS_BITCLK R654 33.4 ACZ_BIT_CLK

C759
27pF/50V_4



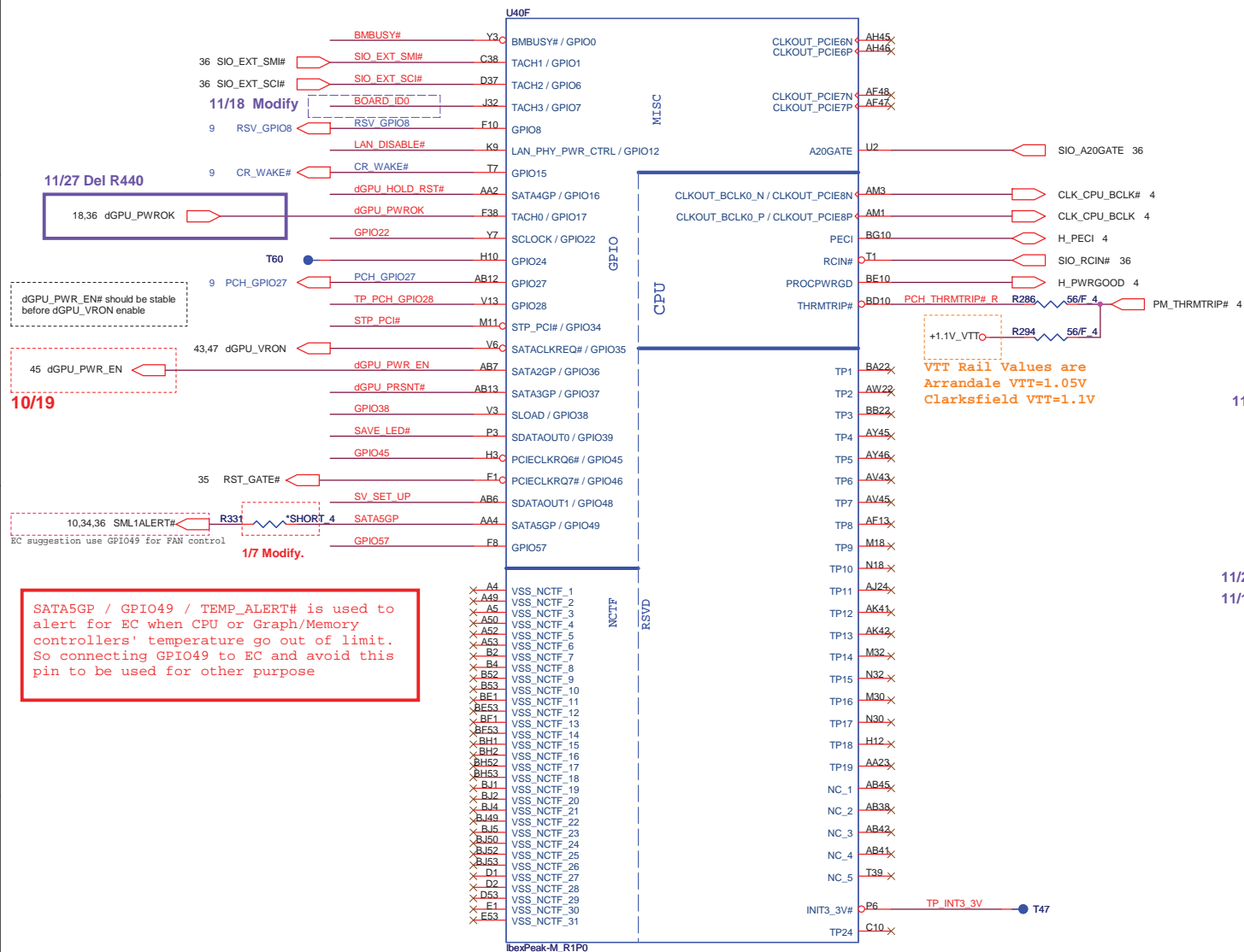
The diagram illustrates the IBEX PEAK-M 3/6 system, showing various components and their connections. The top section details the main board ID, including components like the CPU, memory, storage, and peripheral interfaces. The bottom section shows the system board ID, including components like the CPU, memory, storage, and peripheral interfaces. The diagram is labeled with various components and their connections, including a table of components and their values.

Table 1: Components and Values

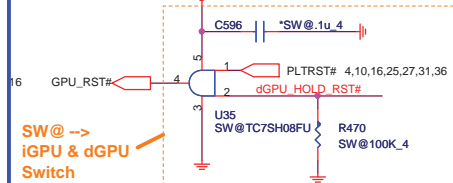
Component	Value
USB OC7#	6
USB OC8#	7
USB OC9#	8
USB OC10#	9
USB OC11#	10
PCI PIRQ0#	6
PCI PIRQ1#	7
PCI PIRQ2#	8
PCI PIRQ3#	9
PCI PIRQ4#	10
PCI PIRQ5#	11
PCI PIRQ6#	12
PCI PIRQ7#	13
PCI PIRQ8#	14
PCI PIRQ9#	15
PCI PIRQ10#	16
PCI PIRQ11#	17
PCI PIRQ12#	18
PCI PIRQ13#	19
PCI PIRQ14#	20
PCI PIRQ15#	21
PCI PIRQ16#	22
PCI PIRQ17#	23
PCI PIRQ18#	24
PCI PIRQ19#	25
PCI PIRQ20#	26
PCI PIRQ21#	27
PCI PIRQ22#	28
PCI PIRQ23#	29
PCI PIRQ24#	30
PCI PIRQ25#	31
PCI PIRQ26#	32
PCI PIRQ27#	33
PCI PIRQ28#	34
PCI PIRQ29#	35
PCI PIRQ30#	36
PCI PIRQ31#	37
PCI PIRQ32#	38
PCI PIRQ33#	39
PCI PIRQ34#	40
PCI PIRQ35#	41
PCI PIRQ36#	42
PCI PIRQ37#	43
PCI PIRQ38#	44
PCI PIRQ39#	45
PCI PIRQ40#	46
PCI PIRQ41#	47
PCI PIRQ42#	48
PCI PIRQ43#	49
PCI PIRQ44#	50
PCI PIRQ45#	51
PCI PIRQ46#	52
PCI PIRQ47#	53
PCI PIRQ48#	54
PCI PIRQ49#	55
PCI PIRQ50#	56
PCI PIRQ51#	57
PCI PIRQ52#	58
PCI PIRQ53#	59
PCI PIRQ54#	60
PCI PIRQ55#	61
PCI PIRQ56#	62
PCI PIRQ57#	63
PCI PIRQ58#	64
PCI PIRQ59#	65
PCI PIRQ60#	66
PCI PIRQ61#	67
PCI PIRQ62#	68
PCI PIRQ63#	69
PCI PIRQ64#	70
PCI PIRQ65#	71
PCI PIRQ66#	72
PCI PIRQ67#	73
PCI PIRQ68#	74
PCI PIRQ69#	75
PCI PIRQ70#	76
PCI PIRQ71#	77
PCI PIRQ72#	78
PCI PIRQ73#	79
PCI PIRQ74#	80
PCI PIRQ75#	81
PCI PIRQ76#	82
PCI PIRQ77#	83
PCI PIRQ78#	84
PCI PIRQ79#	85
PCI PIRQ80#	86
PCI PIRQ81#	87
PCI PIRQ82#	88
PCI PIRQ83#	89
PCI PIRQ84#	90
PCI PIRQ85#	91
PCI PIRQ86#	92
PCI PIRQ87#	93
PCI PIRQ88#	94
PCI PIRQ89#	95
PCI PIRQ90#	96
PCI PIRQ91#	97
PCI PIRQ92#	98
PCI PIRQ93#	99
PCI PIRQ94#	100
PCI PIRQ95#	101
PCI PIRQ96#	102
PCI PIRQ97#	103
PCI PIRQ98#	104
PCI PIRQ99#	105
PCI PIRQ100#	106
PCI PIRQ101#	107
PCI PIRQ102#	108
PCI PIRQ103#	109
PCI PIRQ104#	110
PCI PIRQ105#	111
PCI PIRQ106#	112
PCI PIRQ107#	113
PCI PIRQ108#	114
PCI PIRQ109#	115
PCI PIRQ110#	116
PCI PIRQ111#	117
PCI PIRQ112#	118
PCI PIRQ113#	119
PCI PIRQ114#	120
PCI PIRQ115#	121
PCI PIRQ116#	122
PCI PIRQ117#	123
PCI PIRQ118#	124
PCI PIRQ119#	125
PCI PIRQ120#	126
PCI PIRQ121#	127
PCI PIRQ122#	128
PCI PIRQ123#	129
PCI PIRQ124#	130
PCI PIRQ125#	131
PCI PIRQ126#	132
PCI PIRQ127#	133
PCI PIRQ128#	134
PCI PIRQ129#	135
PCI PIRQ130#	136
PCI	

IV@ --> iGPU only
 EV@ --> dGPU only
 SW@ --> iGPU & dGPU Switch
 ES@ --> External VGA SKU

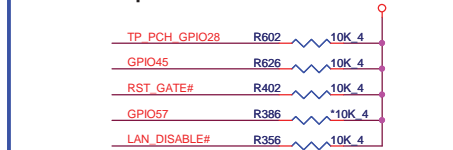
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



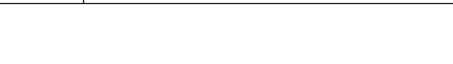
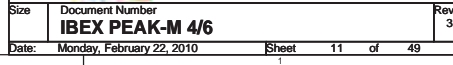
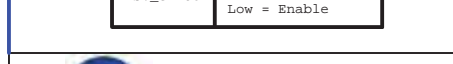
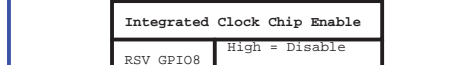
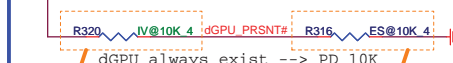
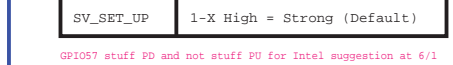
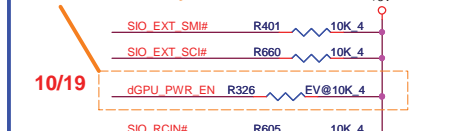
GPU RST#



GPIO Pull-up/Pull-down



EV@ --> dGPU only



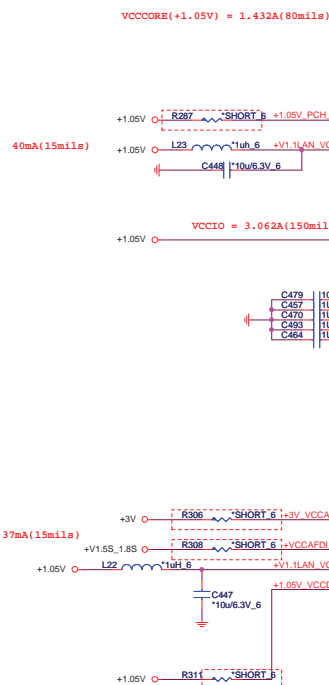
Integrated Clock Chip Enable

RSV_GPIO8	High = Disable
	Low = Enable

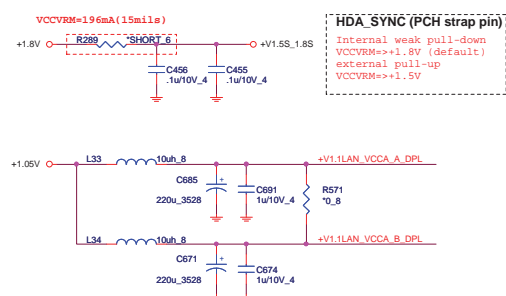
Quanta Computer Inc.
PROJECT : ZR7

IBEX PEAK-M (POWER)

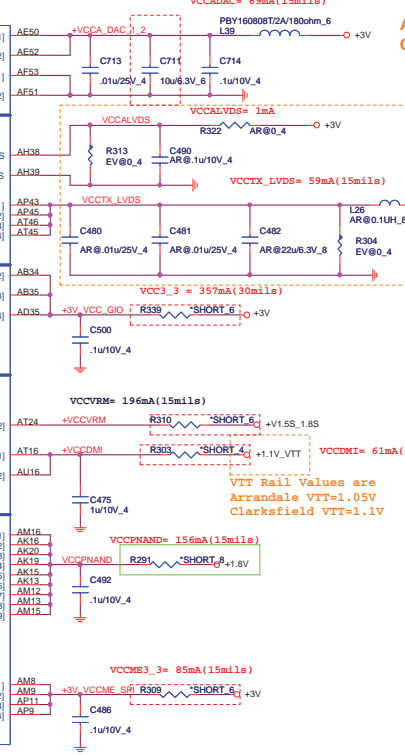
AR@ --> ARD CPU
CF@ --> CFD CPU



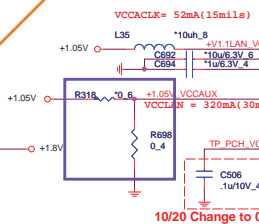
```
VRM enable by strap pin GPIO27
which supply clean 1.05V for
[VCCAC1LK, VCCAP1LEXP, VCCED1PLJ, VCCSATAP1LJ]
```



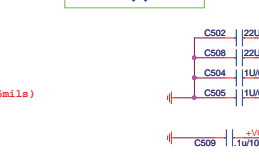
VTT Rail Values are
Arrandale VTT=1.05V
Clarksfield VTT=1.1V



AR@ --> ARD CPU
CF@ --> CFD CPU



VCCME(+1.05V) = 1.849A(100mils)



VCCSUS3_3 = 163mA(20mils)

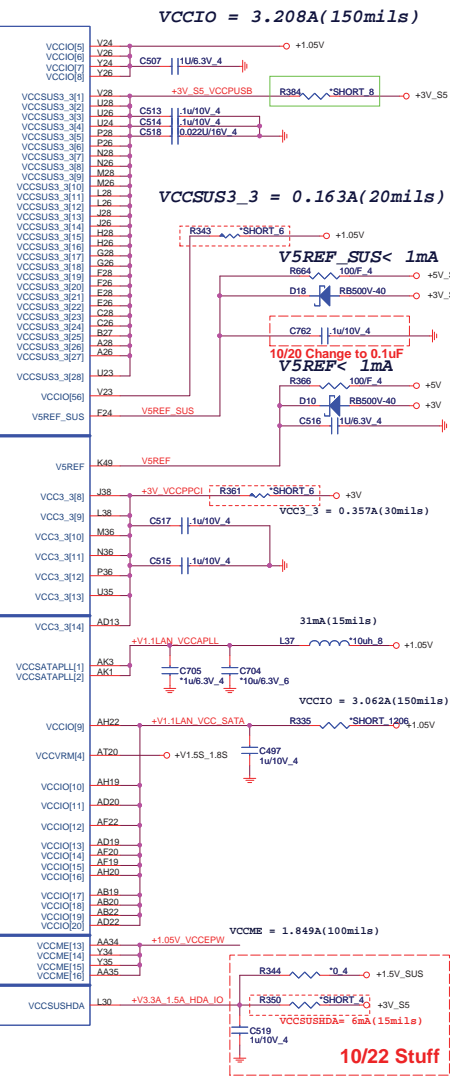
+3V_S5 R378 *SHORT 6 +3V_S5 VCC

VCC3_3 = 0.357A(30mils)

V_CPU_IO >1mA(15mils) C503 .1u/10V_4

+VCCRTC

POWER



10/22 Stuff



Quanta Computer Inc.
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	IBEX PEAK-M 5/6	
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IBEX PEAK-M (GND)

U40H		
AB16	VSS[0]	
AA19	VSS[1]	VSS[80] AK30
AA20	VSS[2]	VSS[81] AK31
AA22	VSS[3]	VSS[82] AK32
AM19	VSS[4]	VSS[83] AK34
AA24	VSS[5]	VSS[84] AK35
AA26	VSS[6]	VSS[85] AK38
AA28	VSS[7]	VSS[86] AK43
AA30	VSS[8]	VSS[87] AK46
AA31	VSS[9]	VSS[88] AK49
AA32	VSS[10]	VSS[89] AK5
AB11	VSS[11]	VSS[90] AK8
AB15	VSS[12]	VSS[91] AL2
AB23	VSS[13]	VSS[92] AM11
AB31	VSS[14]	VSS[93] BB44
AB32	VSS[15]	VSS[94] AD24
AB39	VSS[16]	VSS[95] AM20
AB43	VSS[17]	VSS[96] AM22
AB47	VSS[18]	VSS[97] AM24
AB5	VSS[19]	VSS[98] AM26
AB8	VSS[20]	VSS[99] AM28
AC2	VSS[21]	VSS[100] RA42
AC32	VSS[22]	VSS[101] AM30
AD11	VSS[23]	VSS[102] AM31
AD12	VSS[24]	VSS[103] AM32
AD16	VSS[25]	VSS[104] AM34
AD23	VSS[26]	VSS[105] AM35
AD30	VSS[27]	VSS[106] AM38
AD31	VSS[28]	VSS[107] AM39
AD32	VSS[29]	VSS[108] AM42
AD34	VSS[30]	VSS[109] AU20
AD42	VSS[31]	VSS[110] AU22
AD46	VSS[32]	VSS[111] AV22
AD49	VSS[33]	VSS[112] BF3
AD7	VSS[34]	VSS[113] BF51
AE2	VSS[35]	VSS[114] BG18
AE4	VSS[36]	VSS[115] RG24
AE12	VSS[37]	VSS[116] AN32
Y13	VSS[38]	VSS[117] AN50
AH49	VSS[39]	VSS[118] AN62
AL4	VSS[40]	VSS[119] AP12
AF35	VSS[41]	VSS[120] AP42
AP13	VSS[42]	VSS[121] AP46
AN34	VSS[43]	VSS[122] AP49
AE45	VSS[44]	VSS[123] AP5
AF46	VSS[45]	VSS[124] AP8
AF49	VSS[46]	VSS[125] AR2
AF5	VSS[47]	VSS[126] AR52
AF8	VSS[48]	VSS[127] AT11
AG2	VSS[49]	VSS[128] BA12
AG52	VSS[50]	VSS[129] AH48
AH11	VSS[51]	VSS[130] AT32
AH15	VSS[52]	VSS[131] AT36
AH16	VSS[53]	VSS[132] AT41
AH24	VSS[54]	VSS[133] AT47
AH32	VSS[55]	VSS[134] AT7
AV18	VSS[56]	VSS[135] AV12
AH43	VSS[57]	VSS[136] AV16
AH47	VSS[58]	VSS[137] AV20
AH7	VSS[59]	VSS[138] AV24
AJ19	VSS[60]	VSS[139] AV30
AJ2	VSS[61]	VSS[140] AV34
AJ20	VSS[62]	VSS[141] AV38
AJ22	VSS[63]	VSS[142] AV42
AJ26	VSS[64]	VSS[143] AV46
AJ28	VSS[65]	VSS[144] AV5
AJ32	VSS[66]	VSS[145] AV8
AJ34	VSS[67]	VSS[146] AW14
AT5	VSS[68]	VSS[147] AW18
AK12	VSS[69]	VSS[148] AW2
AM41	VSS[70]	VSS[149] AW32
AN19	VSS[71]	VSS[150] AW36
AK26	VSS[72]	VSS[151] AW40
AK22	VSS[73]	VSS[152] AW52
AK23	VSS[74]	VSS[153] AY11
AK28	VSS[75]	VSS[154] AY43
	VSS[76]	VSS[155] AY47
	VSS[77]	
	VSS[78]	
	VSS[79]	

IbexPeak-M_R1P0

U40I

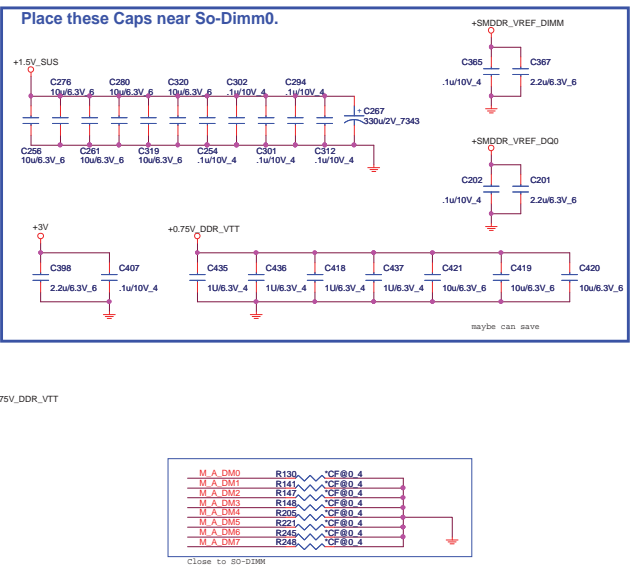
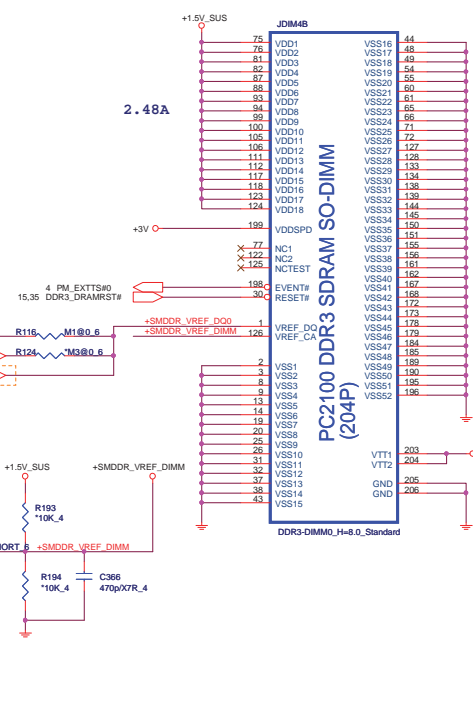
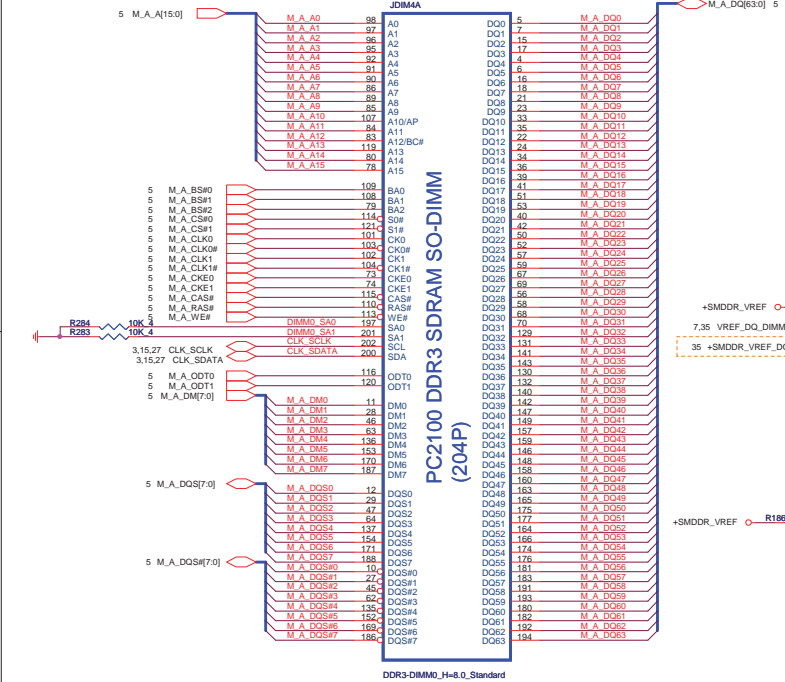
AY7	VSS[159]	VSS[259] H49
B11	VSS[160]	VSS[260] H5
B15	VSS[161]	VSS[261] J24
B19	VSS[162]	VSS[262] K11
B23	VSS[163]	VSS[263] K43
B31	VSS[164]	VSS[264] K47
B35	VSS[165]	VSS[265] L14
B39	VSS[166]	VSS[266] L18
B43	VSS[167]	VSS[267] L2
B47	VSS[168]	VSS[268] L22
B7	VSS[169]	VSS[269] L32
BG12	VSS[170]	VSS[270] L36
BB12	VSS[171]	VSS[271] L40
BB16	VSS[172]	VSS[272] L52
BB20	VSS[173]	VSS[273] M12
BB24	VSS[174]	VSS[274] M16
BB30	VSS[175]	VSS[275] M20
BB34	VSS[176]	VSS[276] M34
BB38	VSS[177]	VSS[277] M38
BB42	VSS[178]	VSS[278] M42
BB49	VSS[179]	VSS[279] M46
BB5	VSS[180]	VSS[280] M49
BC10	VSS[181]	VSS[281] M5
BC14	VSS[182]	VSS[282] M8
BC18	VSS[183]	VSS[283] N24
BC2	VSS[184]	VSS[284] P11
BC22	VSS[185]	VSS[285] AD15
BC32	VSS[186]	VSS[286] P22
BC36	VSS[187]	VSS[287] P30
BC40	VSS[188]	VSS[288] P32
BC44	VSS[189]	VSS[289] P34
BC52	VSS[190]	VSS[290] P42
BH9	VSS[191]	VSS[291] P46
BD48	VSS[192]	VSS[292] P47
BD49	VSS[193]	VSS[293] R2
BD5	VSS[194]	VSS[294] R52
BE12	VSS[195]	VSS[295] T12
BE16	VSS[196]	VSS[296] T41
BE20	VSS[197]	VSS[297] T46
BE24	VSS[198]	VSS[298] T49
BE30	VSS[199]	VSS[299] T5
BE34	VSS[200]	VSS[300] T8
BE38	VSS[201]	VSS[301] U30
BE42	VSS[202]	VSS[302] U32
BE46	VSS[203]	VSS[303] U34
BE50	VSS[204]	VSS[304] V11
BE6	VSS[205]	VSS[305] V19
BE8	VSS[206]	VSS[306] V20
BF3	VSS[207]	VSS[307] V22
BF51	VSS[208]	VSS[308] V30
BG18	VSS[209]	VSS[309] V31
RG24	VSS[210]	VSS[310] V32
AN32	VSS[211]	VSS[311] V34
AN50	VSS[212]	VSS[312] V35
AN62	VSS[213]	VSS[313] V38
AP12	VSS[214]	VSS[314] V43
AP42	VSS[215]	VSS[315] V45
AP46	VSS[216]	VSS[316] V46
AP49	VSS[217]	VSS[317] V47
AP5	VSS[218]	VSS[318] V49
AP8	VSS[219]	VSS[319] V5
AR2	VSS[220]	VSS[320] V8
AR52	VSS[221]	VSS[321] W2
AT11	VSS[222]	VSS[322] W52
BA12	VSS[223]	VSS[323] Y11
AH48	VSS[224]	VSS[324] Y12
AT32	VSS[225]	VSS[325] Y15
AT36	VSS[226]	VSS[326] Y19
AT41	VSS[227]	VSS[327] Y23
AT47	VSS[228]	VSS[328] Y28
AT7	VSS[229]	VSS[329] Y30
AV12	VSS[230]	VSS[330] Y31
AV16	VSS[231]	VSS[331] Y32
AV20	VSS[232]	VSS[332] Y33
AV24	VSS[233]	VSS[333] Y36
AV30	VSS[234]	VSS[334] Y47
AV34	VSS[235]	VSS[335] Y49
AV38	VSS[236]	VSS[336] Y5
AV42	VSS[237]	VSS[337] Y6
AV46	VSS[238]	VSS[338] Y8
AV5	VSS[239]	VSS[339] P24
AV8	VSS[240]	VSS[340] T43
AW14	VSS[241]	VSS[341] AD51
AW18	VSS[242]	VSS[342] ATR
AW2	VSS[243]	VSS[343] AD47
AW32	VSS[244]	VSS[344] Y47
AW36	VSS[245]	VSS[345] AT12
AW40	VSS[246]	VSS[346] AM6
AW52	VSS[247]	VSS[347] AT13
AY11	VSS[248]	VSS[348] AM5
AY43	VSS[249]	VSS[349] AK45
AY47	VSS[250]	VSS[350] AK38
	VSS[251]	VSS[351] AV14
	VSS[252]	
	VSS[253]	
	VSS[254]	
	VSS[255]	
	VSS[256]	
	VSS[257]	
	VSS[258]	

IbexPeak-M_R1P0

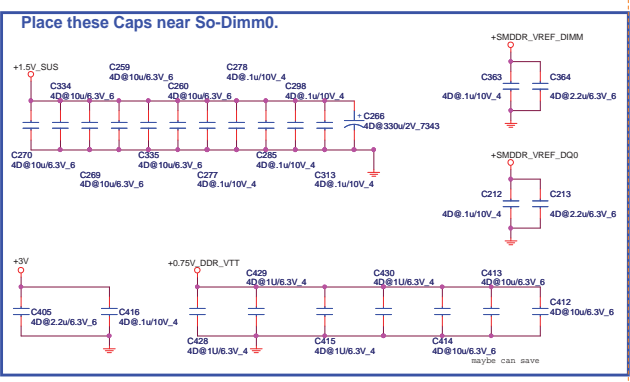
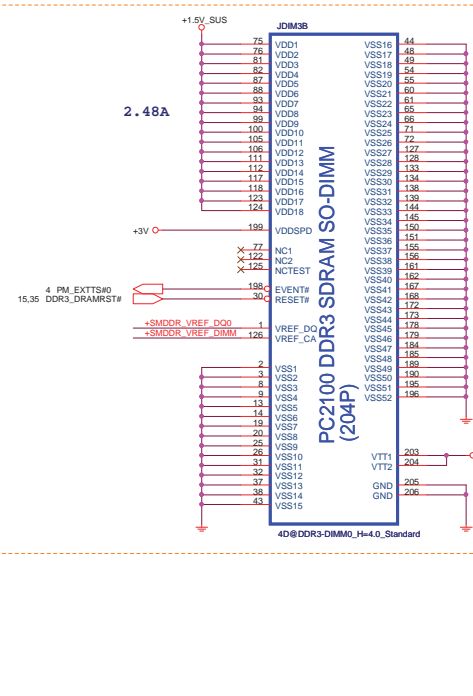
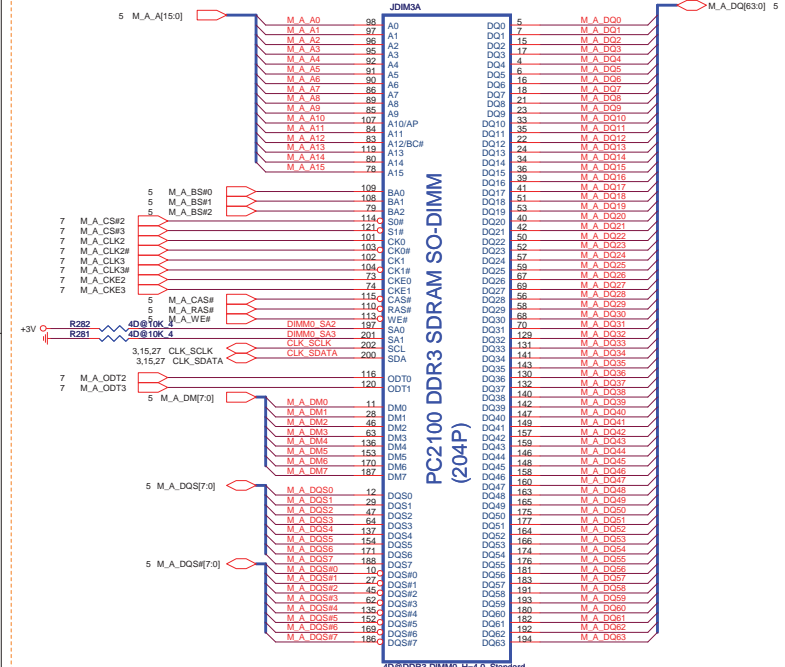


Quanta Computer Inc.
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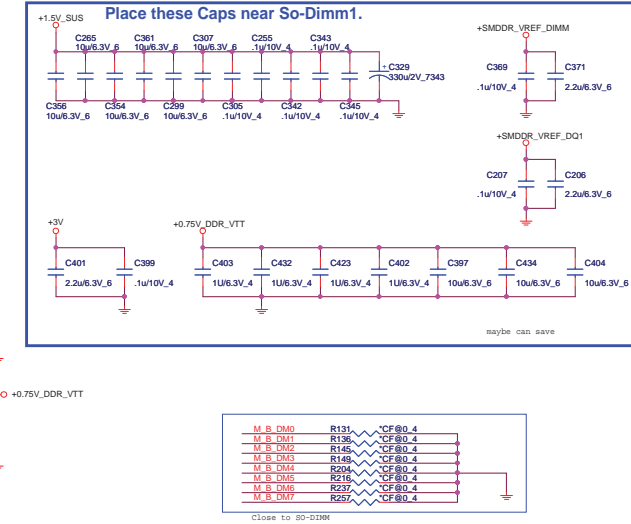
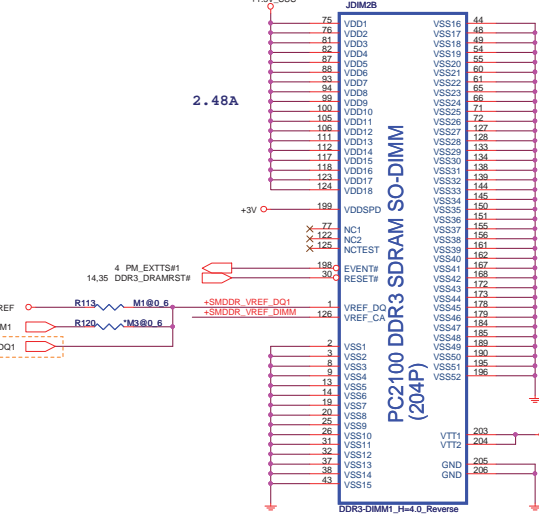
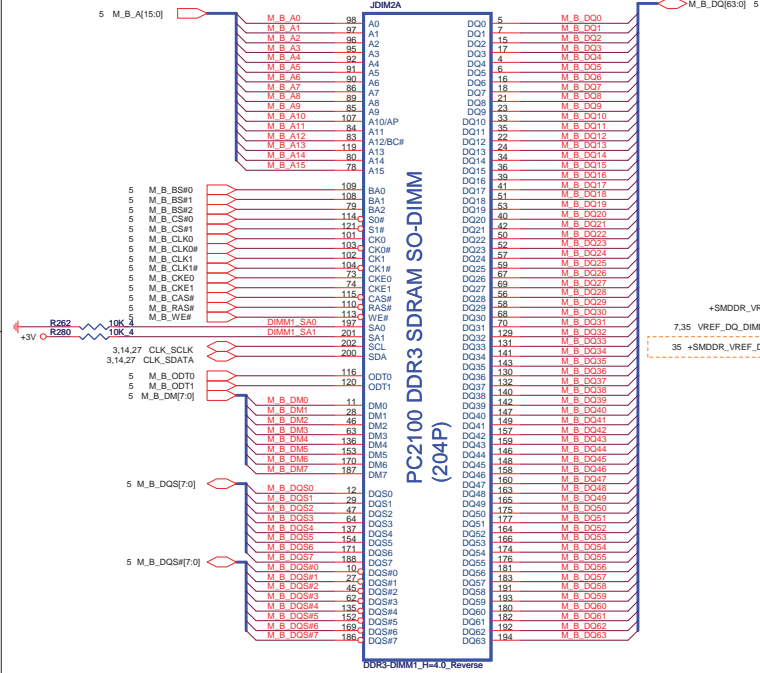
Size	Document Number	Rev
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DIMM A0

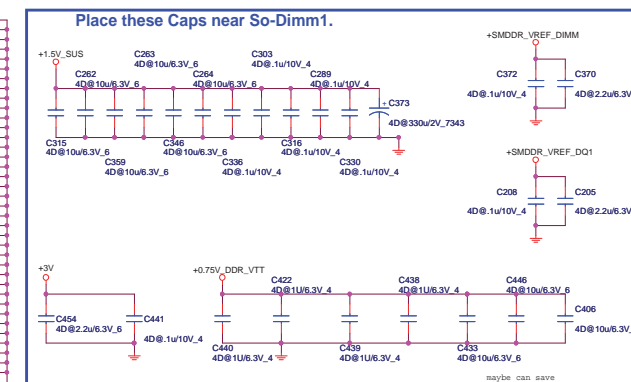
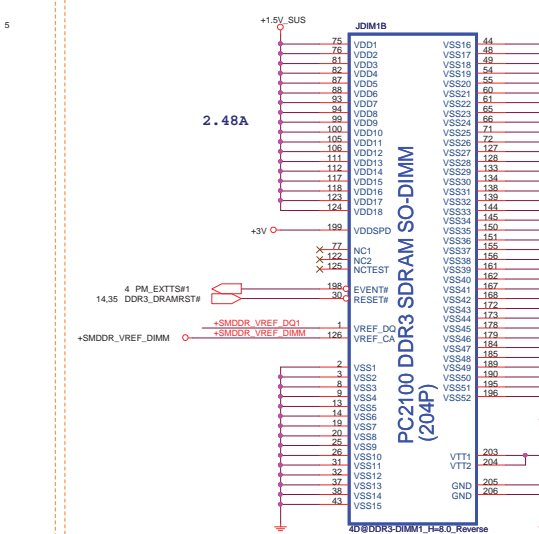
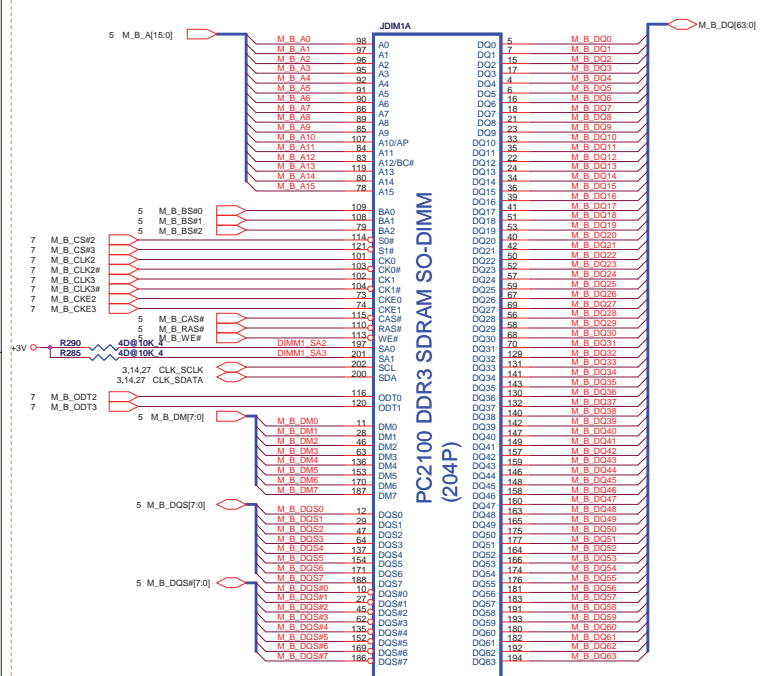
DIMM A1 4D@ --> 4 SO-DIMM



DIMM B0



DIMM B1 4D@ --> 4 SO-DIMM



VSP@ --> Operation P/N (VGA) 11EP@ --> N11P/N11E-GE1 Setting
ES@ --> External VGA SKU U33B 12/1

U33B

12/02 modify
package for N10

21 VMA_DQ[63..0]

21 VMA_DM[7..0]

21 VMA_WDQS[7..0]

21 VMA_RDQS[7..0]

22 VMC_DQ[63..0]

22 VMC_DM[7..0]

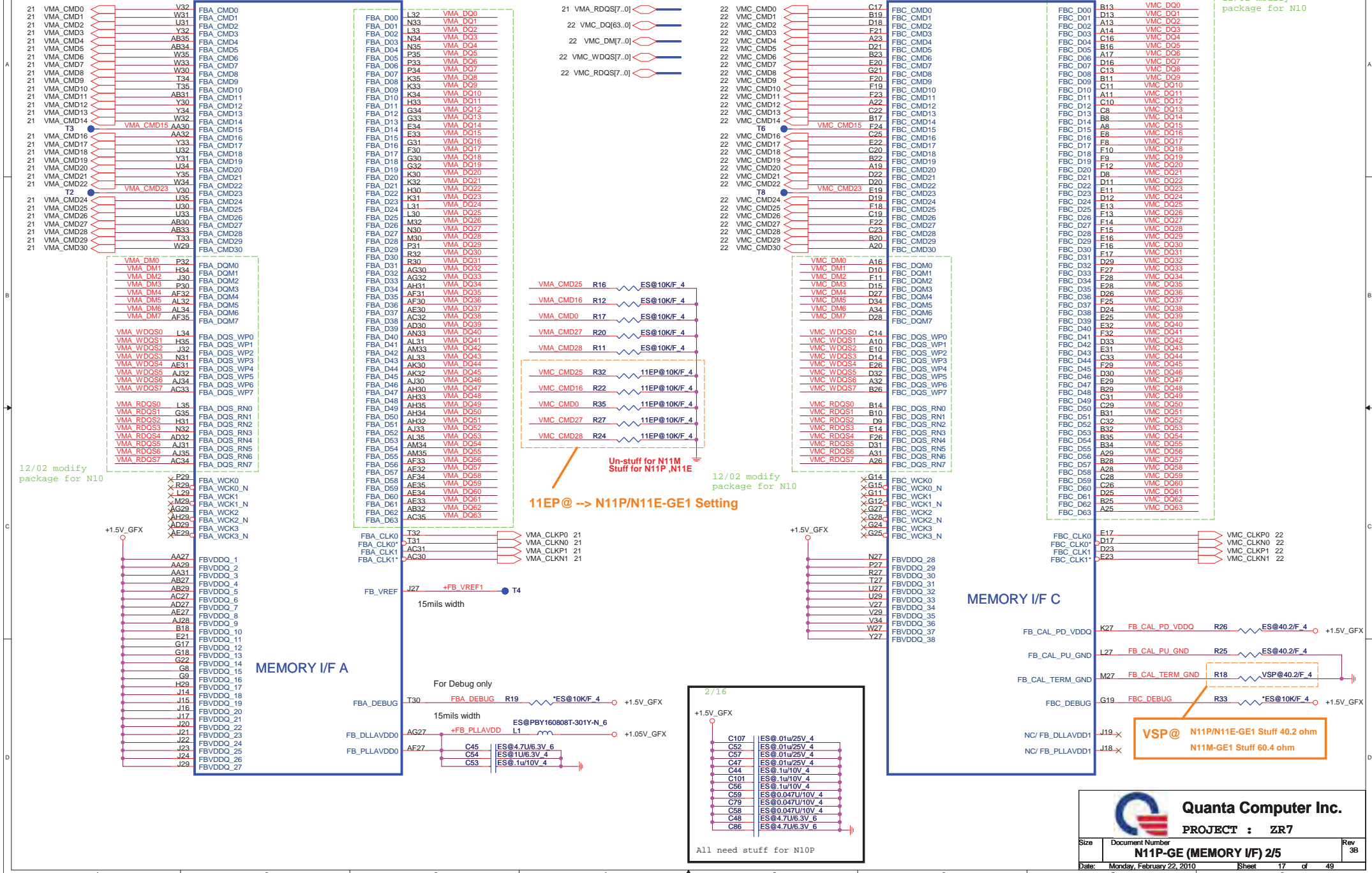
22 VMC_WDQS[7..0]

22 VMC_RDQS[7..0]

U33C

fcbga973-nvidia-n11p-es-a
COMMON

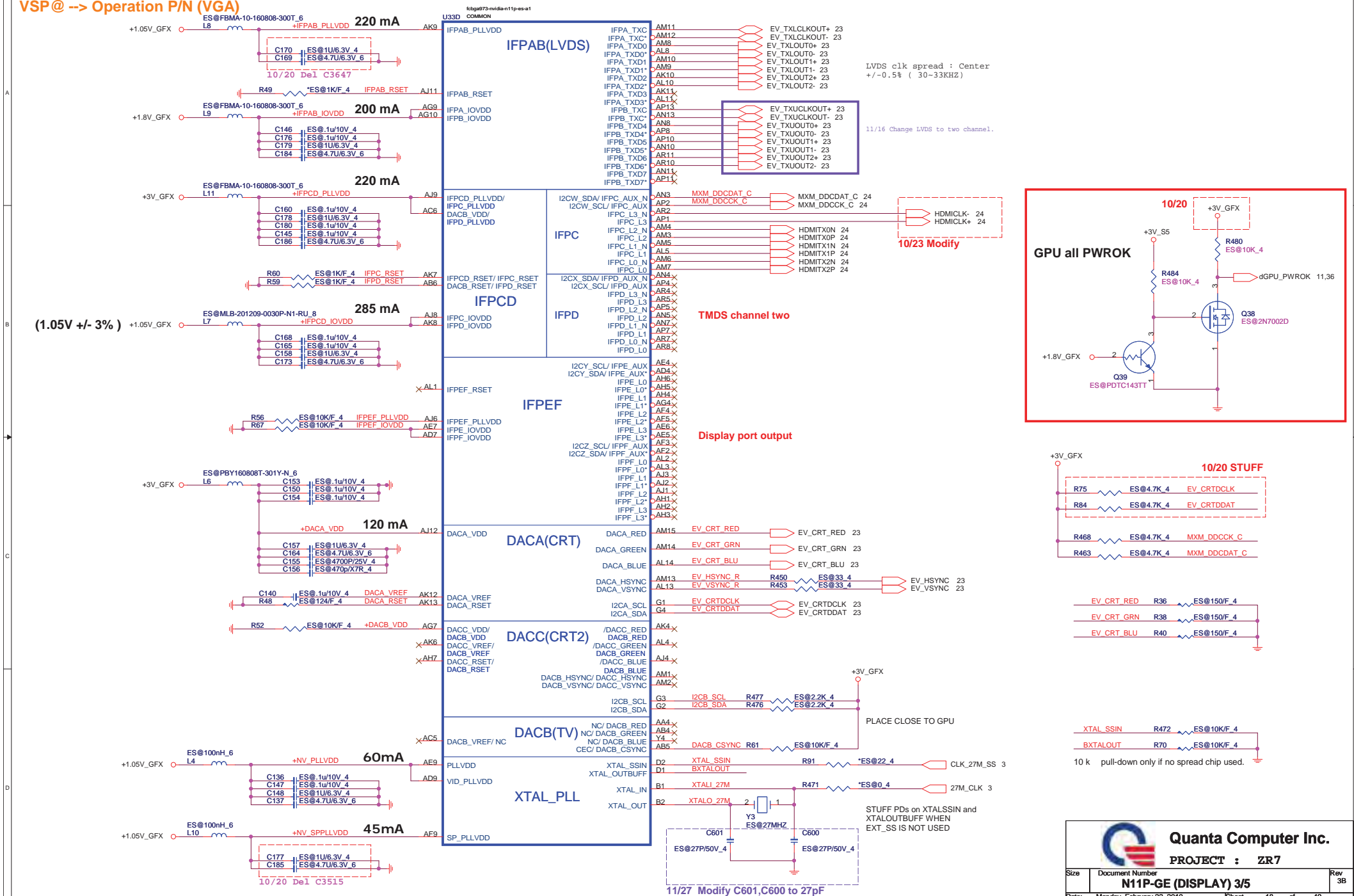
```
12/02 modify
package for N10
```


**Quanta Computer Inc.**

PROJECT : ZR7

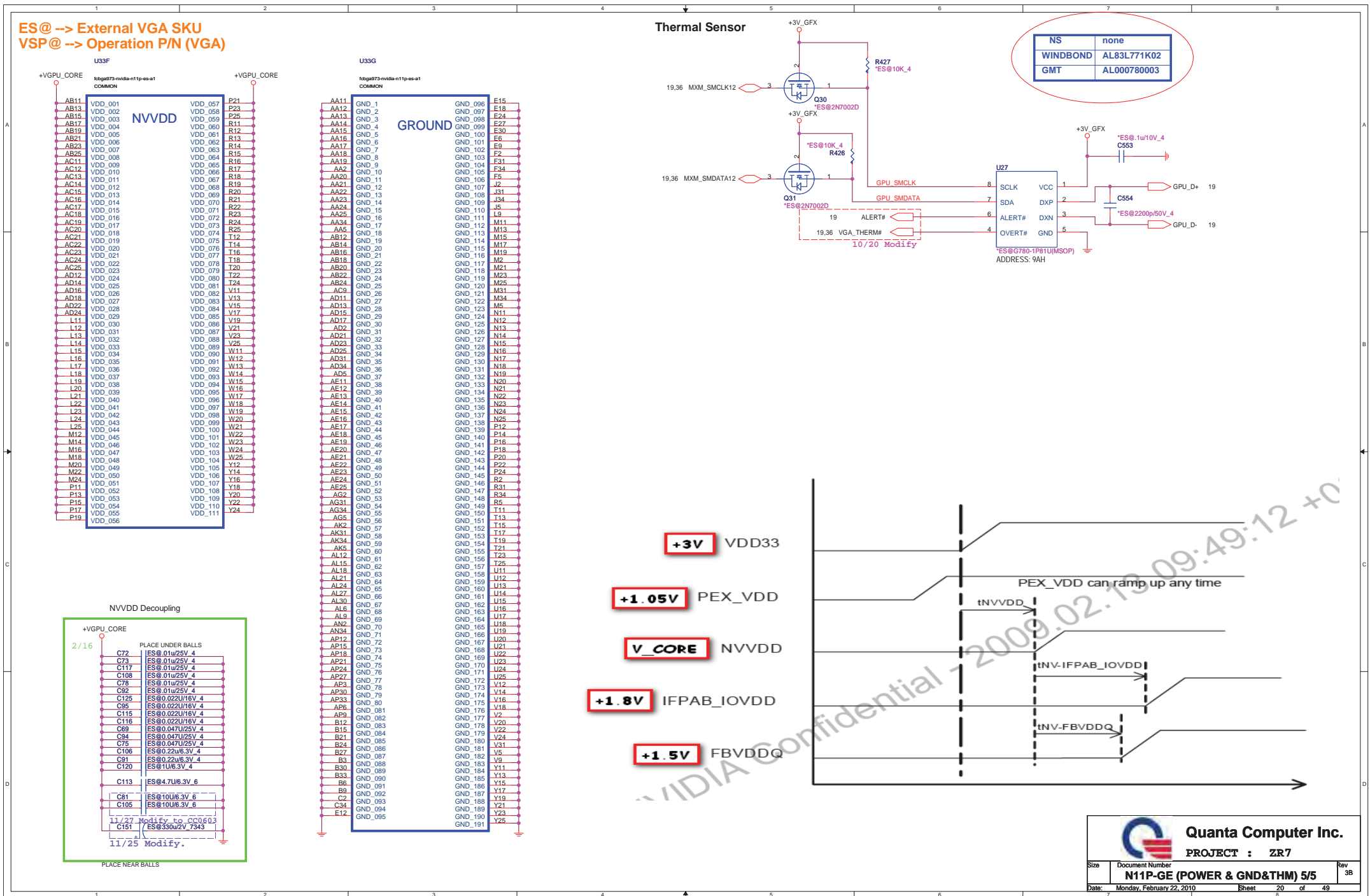
Size	Document Number N11P-GE (MEMORY I/F) 2/5	Rev 3B
Date	Monday, February 22, 2010	Sheet 17 of 49

ES@ --> External VGA SKU
VSP@ --> Operation P/N (VGA)



 <div> <p>Quanta Computer Inc.</p> <p>PROJECT : ZR7</p> </div>		Rev 3
Size	Document Number	
N11P-GE (DISPLAY) 3/5		
Date	Monday, February 22, 2010	Sheet 18 of 40

ES@ --> External VGA SKU
VSP@ --> Operation P/N (VGA)



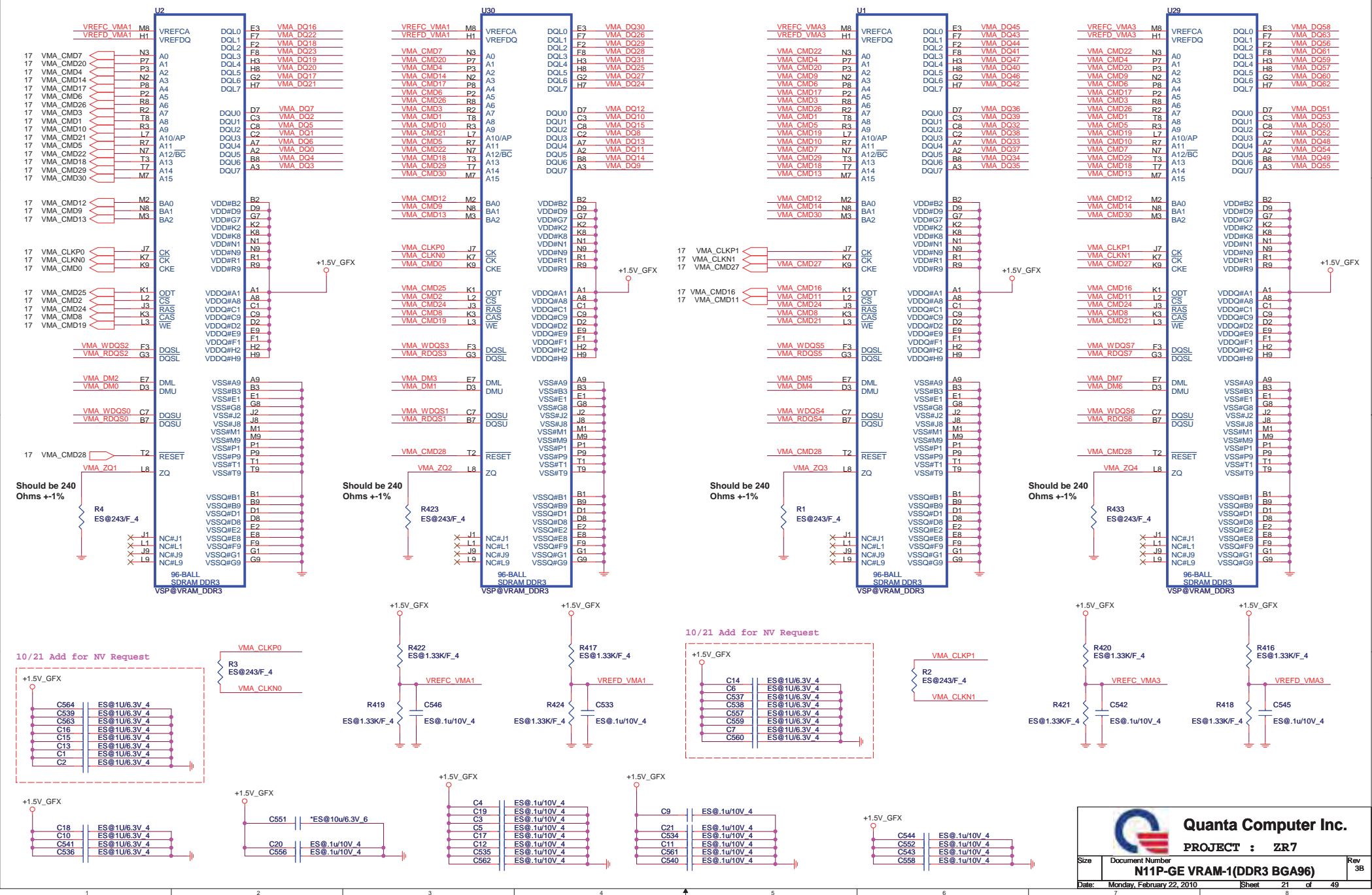
VSP@ --> Operation P/N (VGA-VRAM)

```

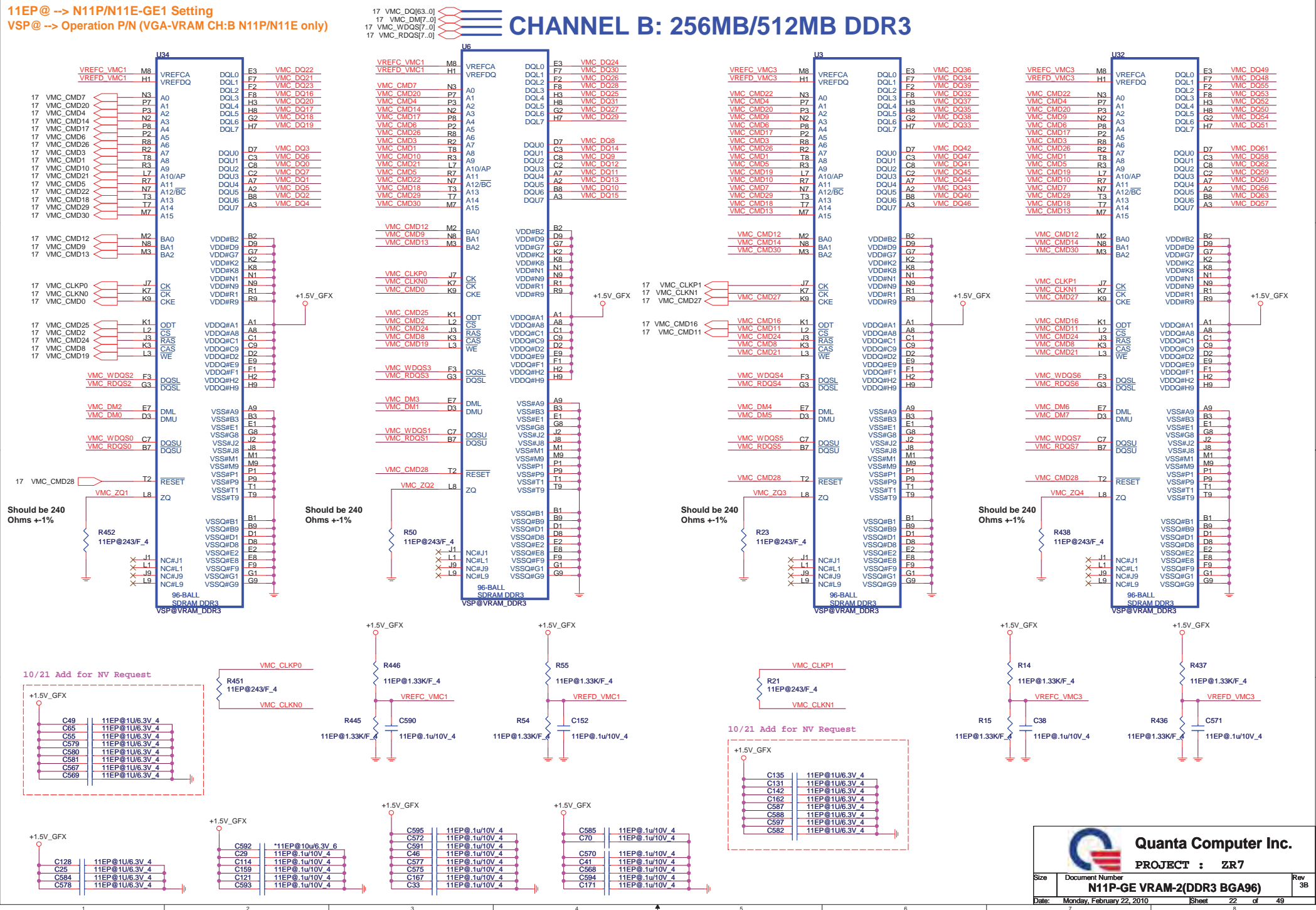
17 VMA_DQ[63..0]
17 VMA_DM[7..0]
17 VMA_WDQS[7..0]
17 VMA_RDQS[7..0]

```

CHANNEL A: 256MB/512MB DDR3



11EP@ --> N11P/N11E-GE1 Setting
VSP@ --> Operation P/N (VGA-VRAM CH:B N11P/N11E only)



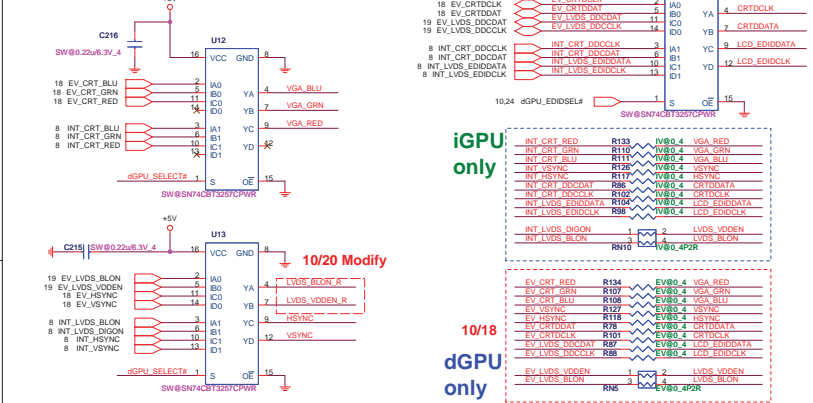
CRT Switch

SW@ -> iGPU & dGPU Switch

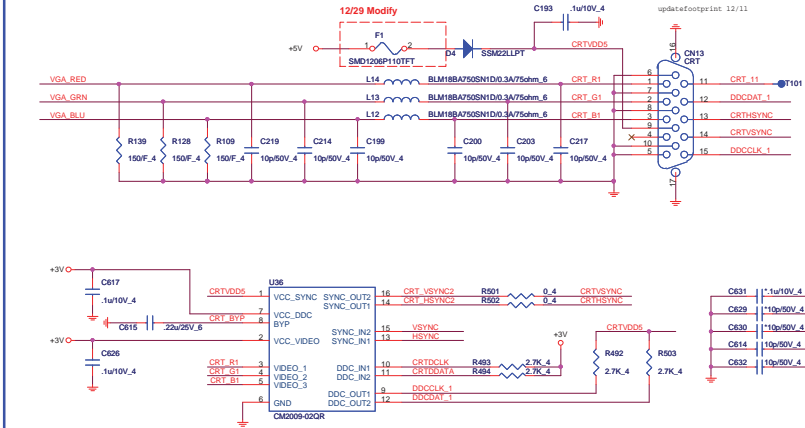
IV@ -> iGPU only

EV@ -> dGPU only

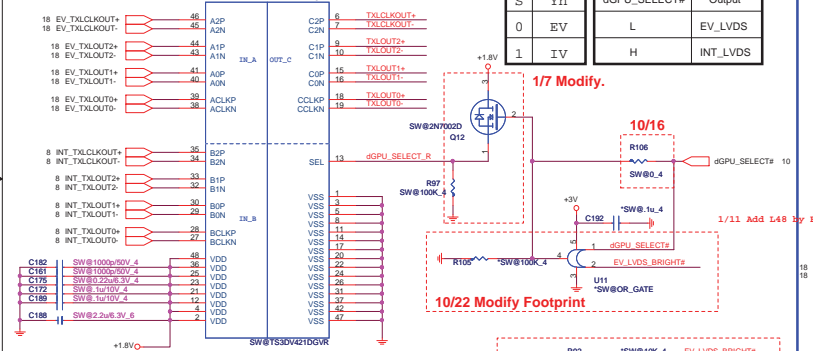
S	Yn	dGPU_SELECT# dGPU_EDIDSEL#	Output
0	EV	L	EV_LVDS/CRT
1	IV	H	INT_LVDS/CRT



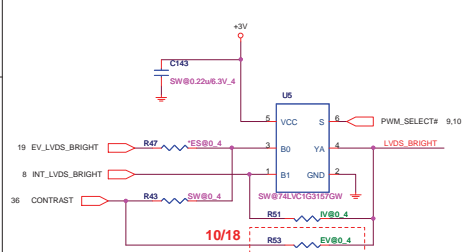
CRT



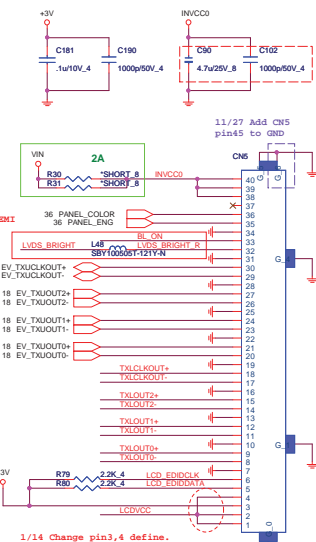
LVDS Switch



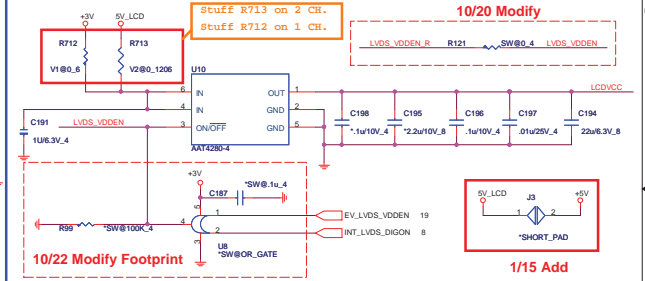
Brightness



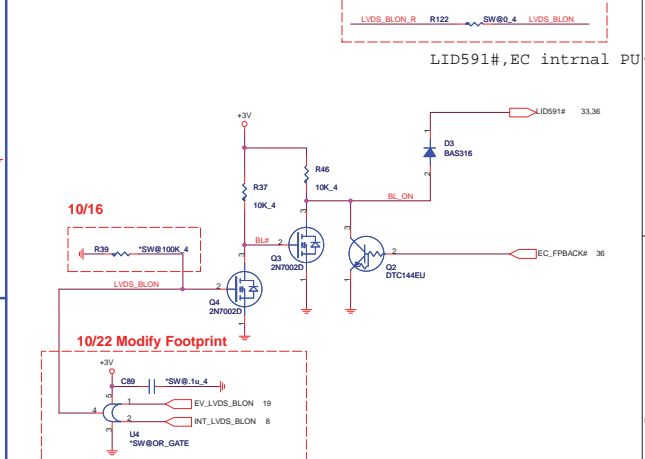
LVDS



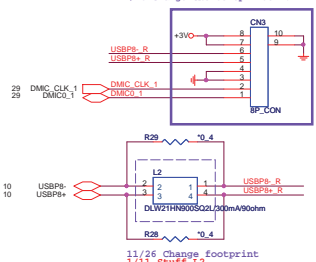
LCD_ON (LCD Power)



Backlight Control

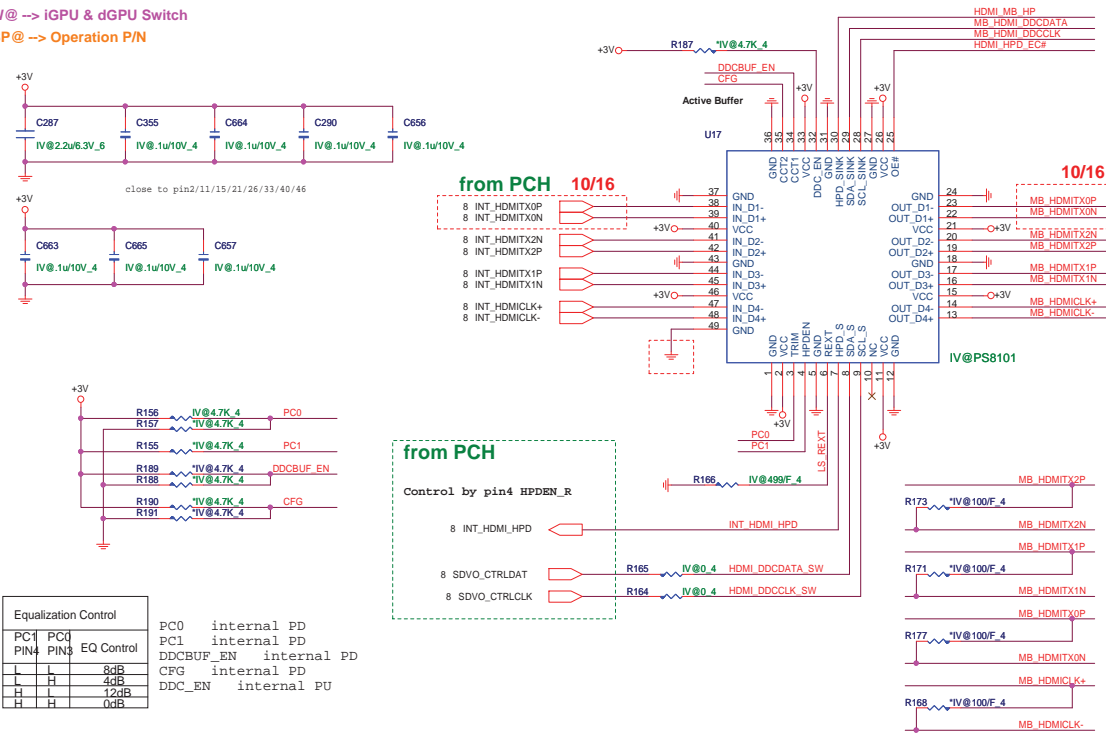


CCD & MIC

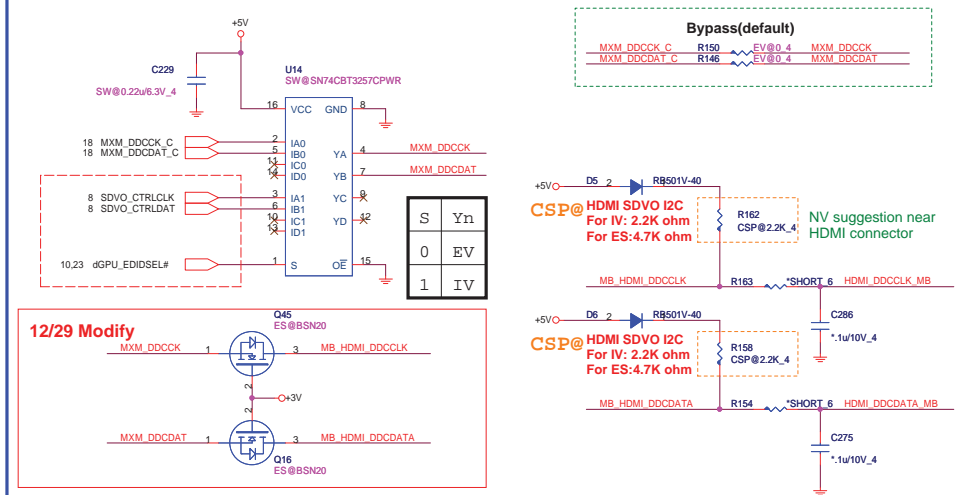


iGPU HDMI LEVEL SHIFTER

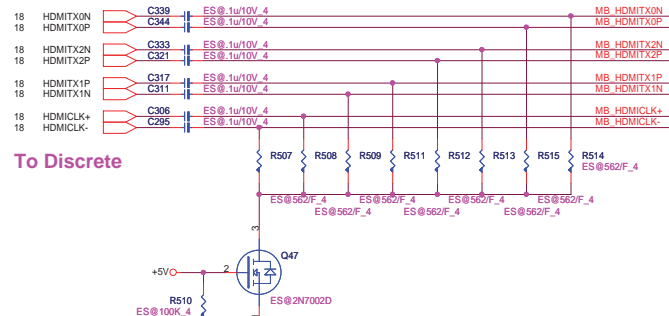
IV@ -> iGPU only
EV@ -> dGPU only
ES@ -> External VGA SKU
SW@ -> iGPU & dGPU Switch
CSP@ -> Operation P/N



SDVO I2C Control



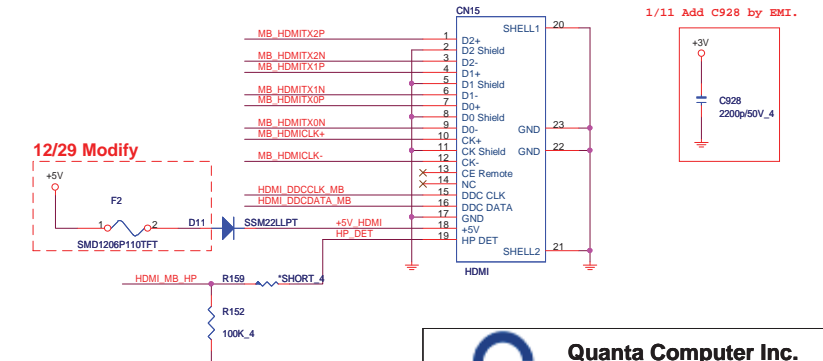
GPU Switchable Graphic HDMI source



ESD Protect

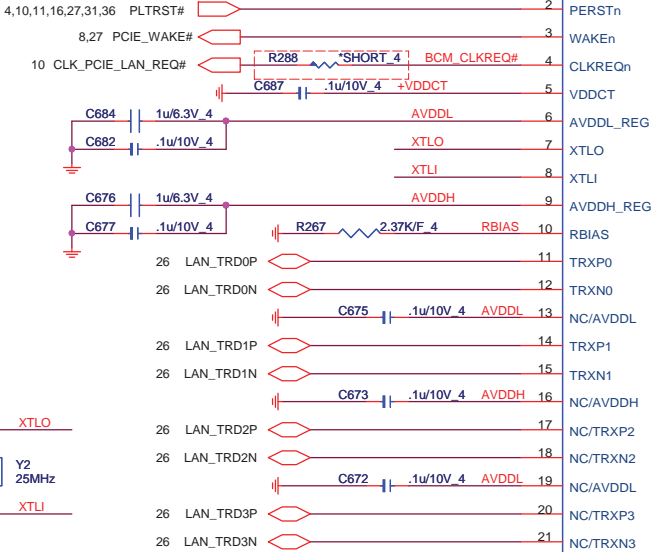
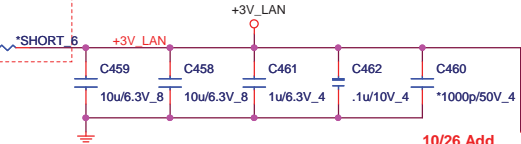
12/29 Delete U15, U16, U18.

HDMI connector

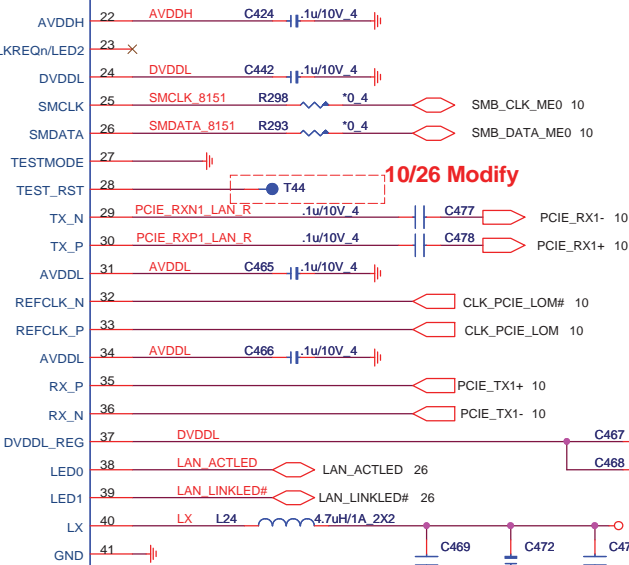


Giga-LAN AR8151

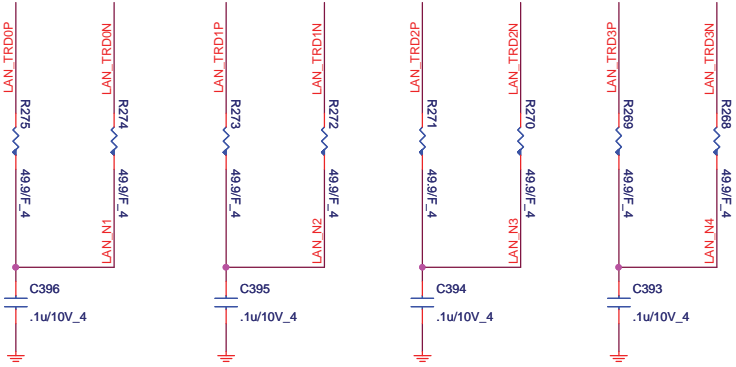
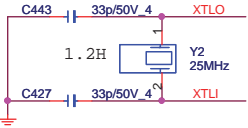
10/26 Add




AR8151
5X5mm
40-Pin QFN



10/26 Modify





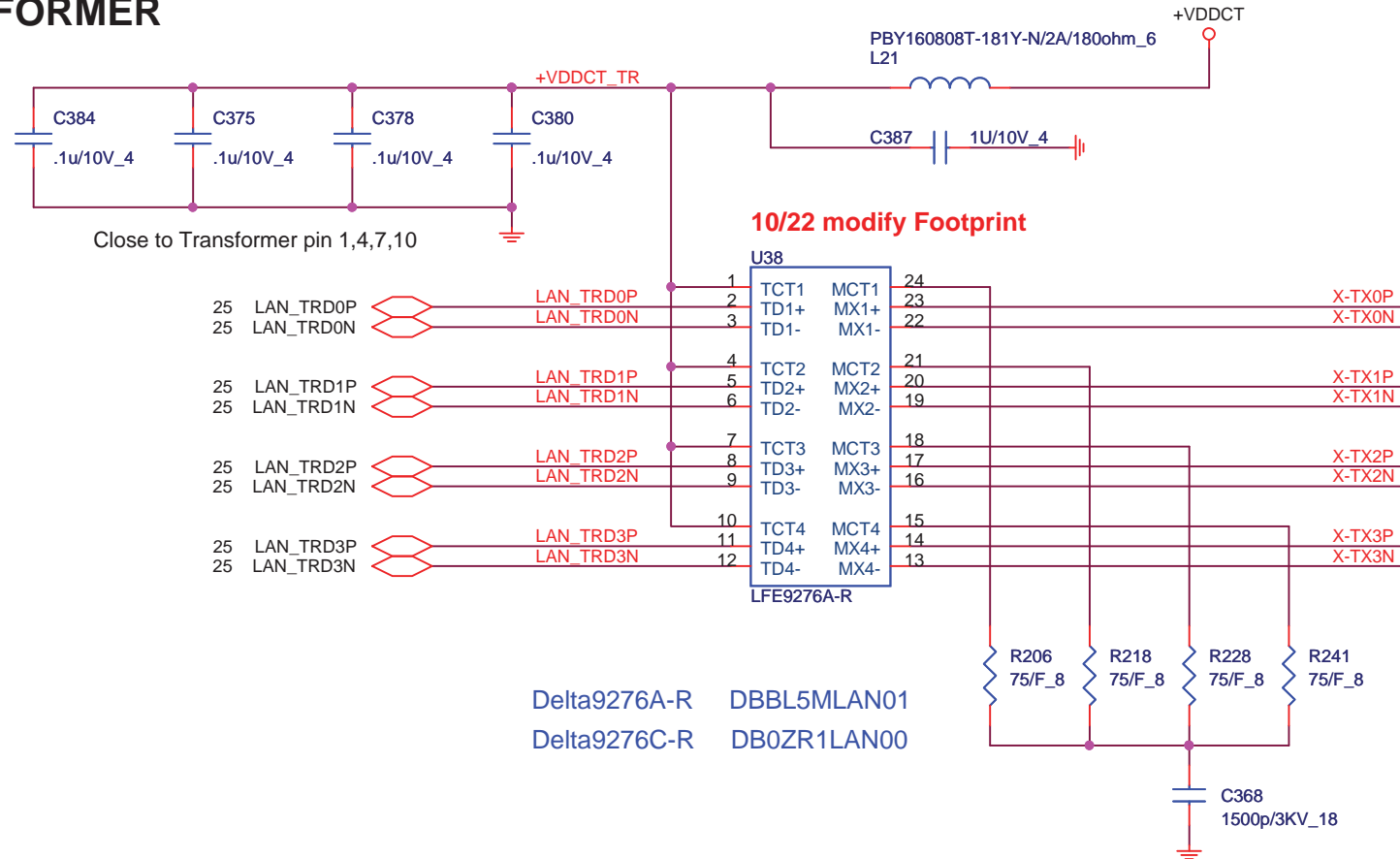
Quanta Computer Inc.

PROJECT : ZR7

GLAN BCM57780

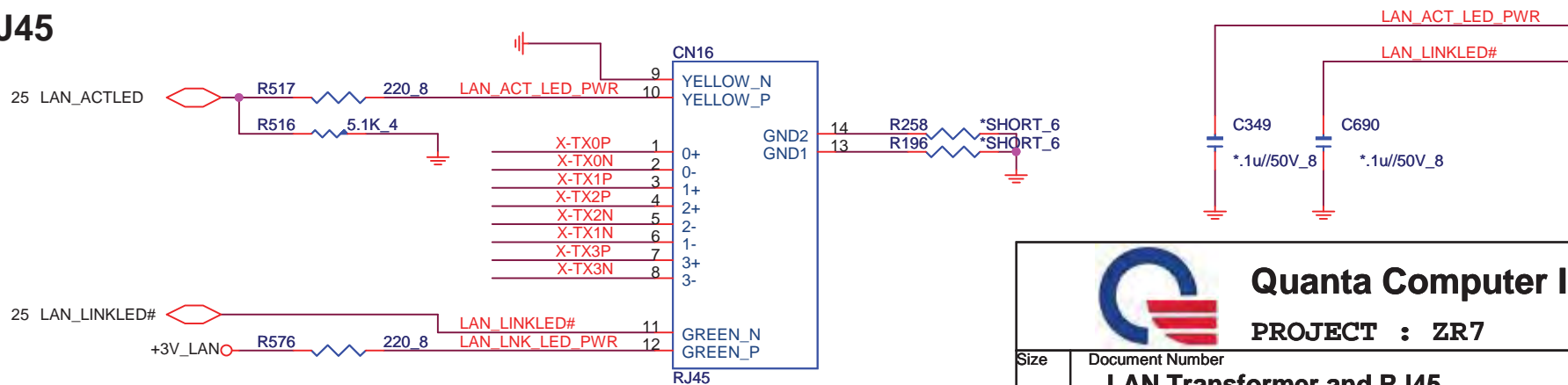
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TRANSFORMER



Delta9276A-R DBBL5MLAN01
Delta9276C-R DB0ZR1LAN00

RJ45



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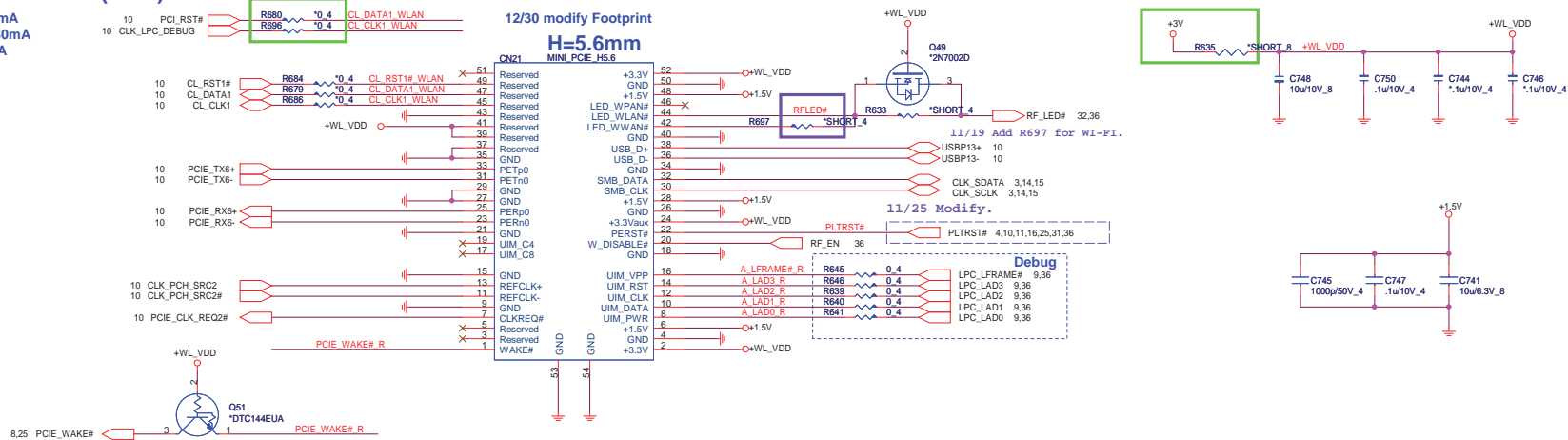
Size	Document Number	Rev
	LAN Transformer and RJ45	3B

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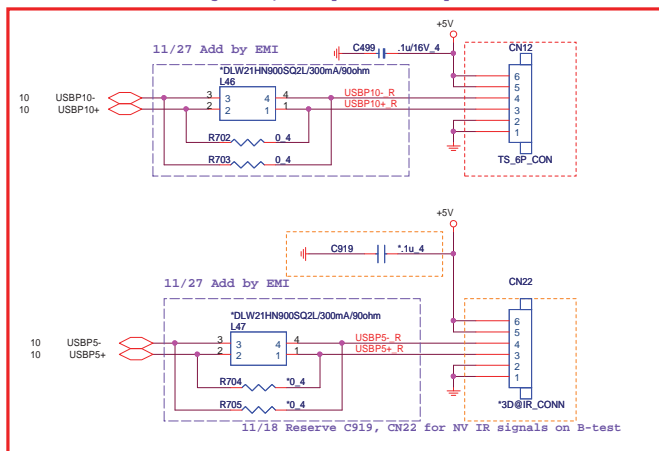
+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

12/30 modify Footprint

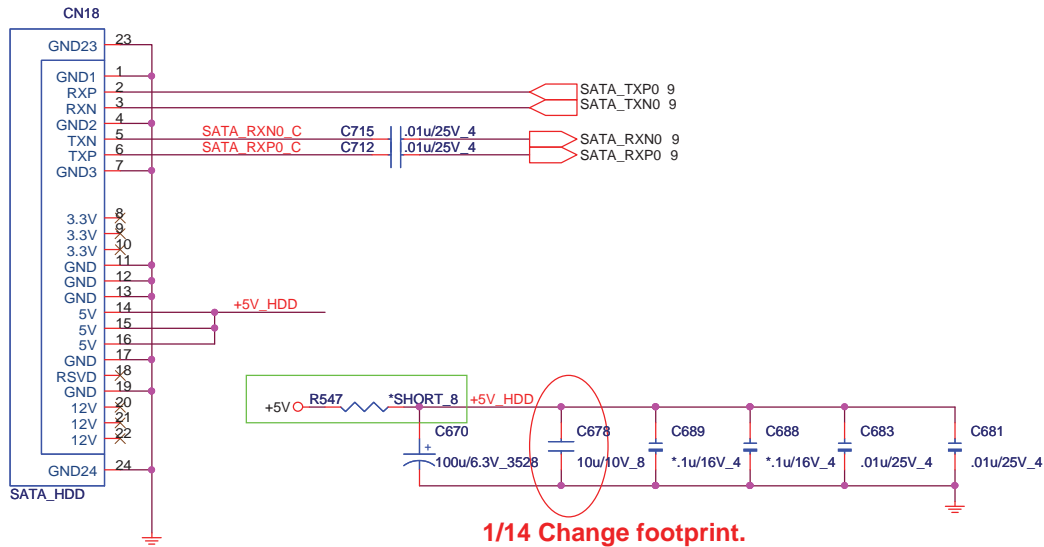
H=5.6mm



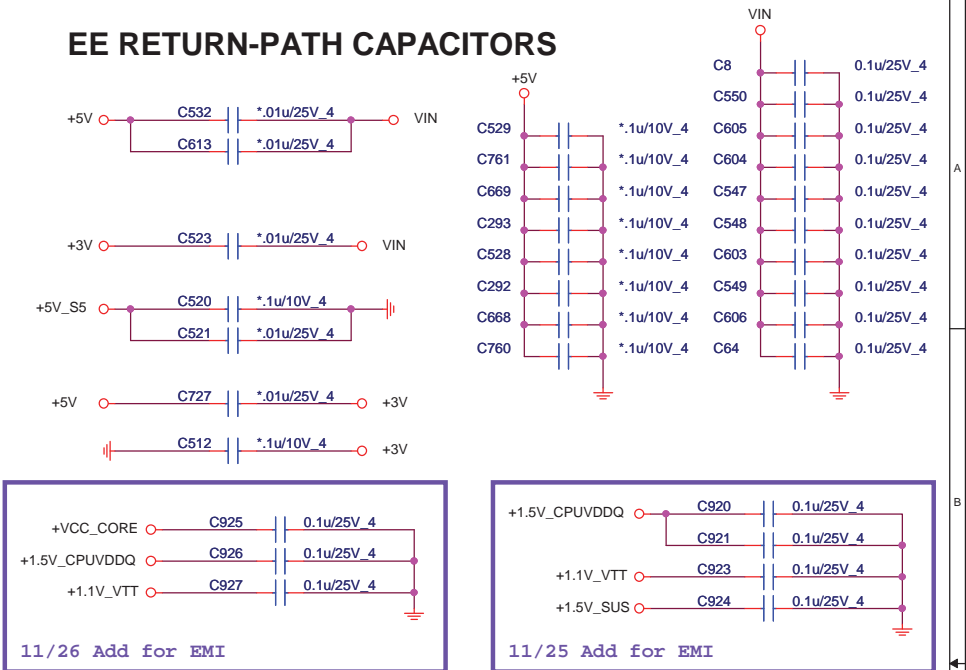
1/8 Change CN12,CN22 6pin conn footprint for Touch Screen.



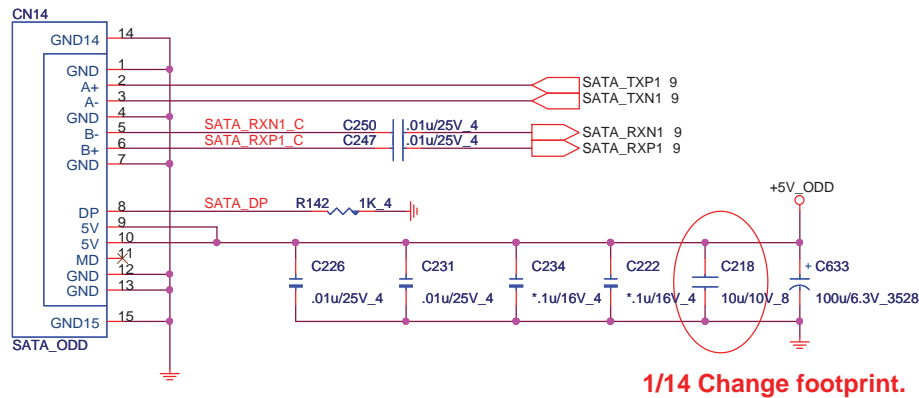
MAIN SATA HDD



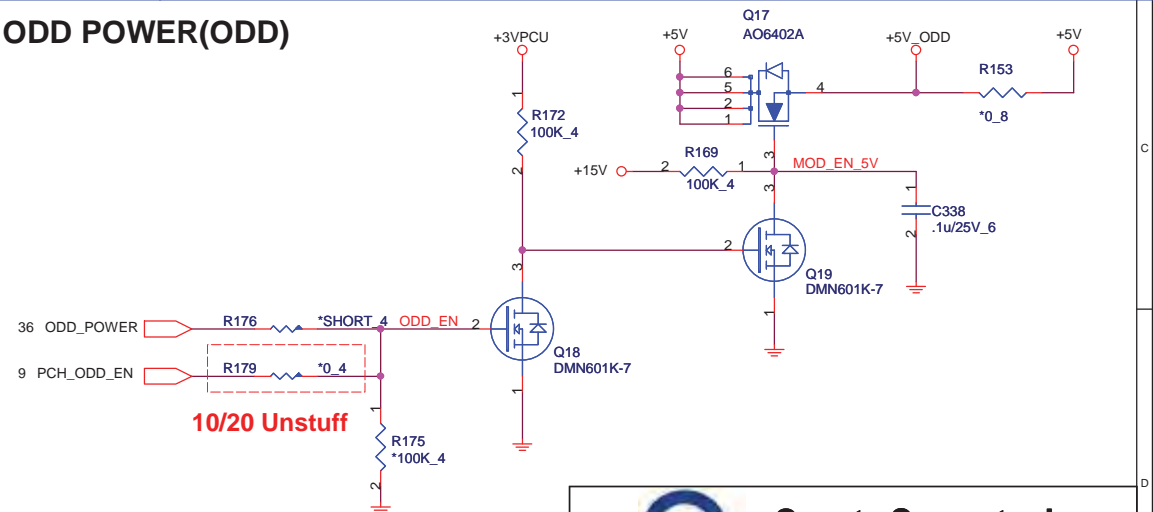
EE RETURN-PATH CAPACITORS



ODD (SATA)

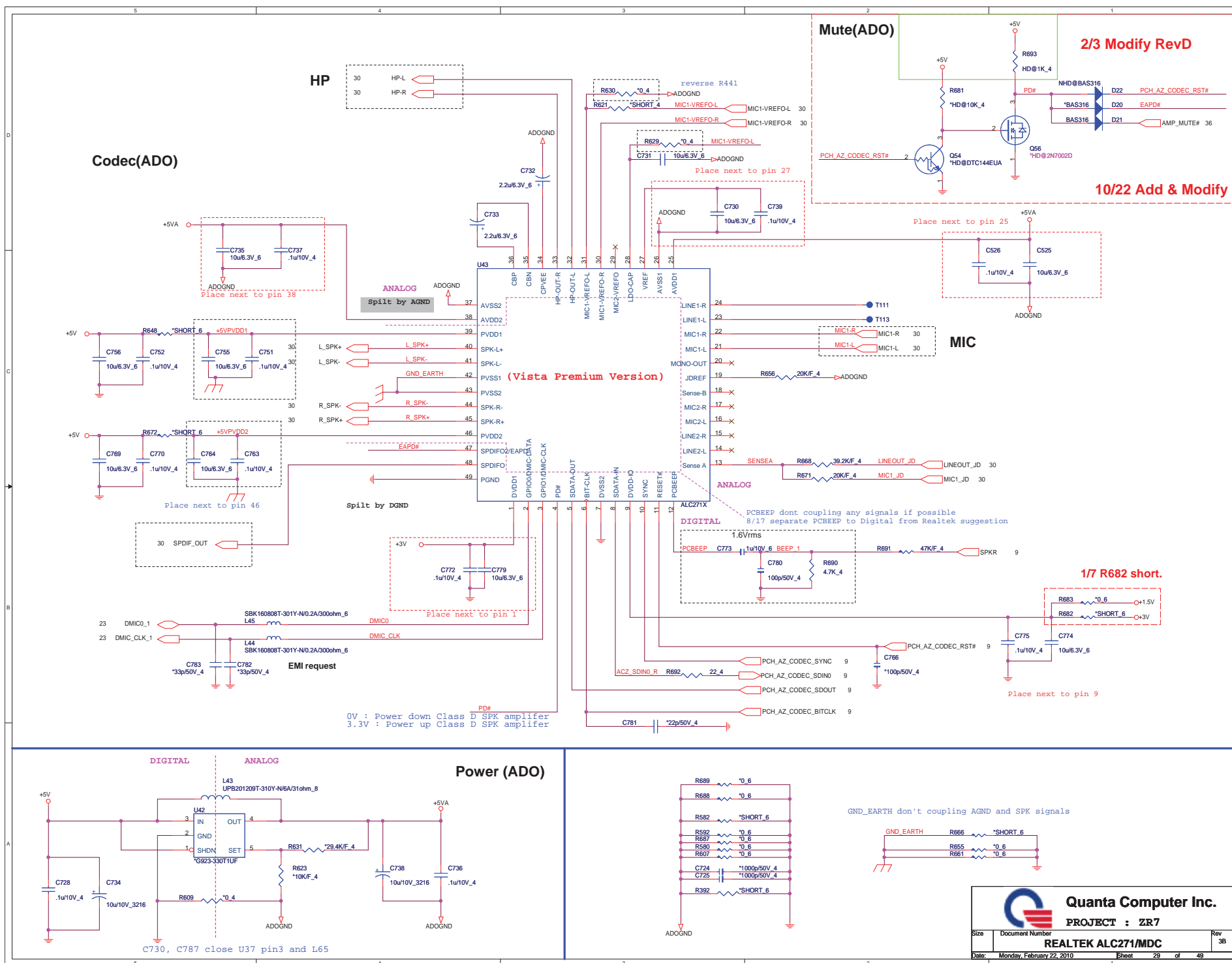


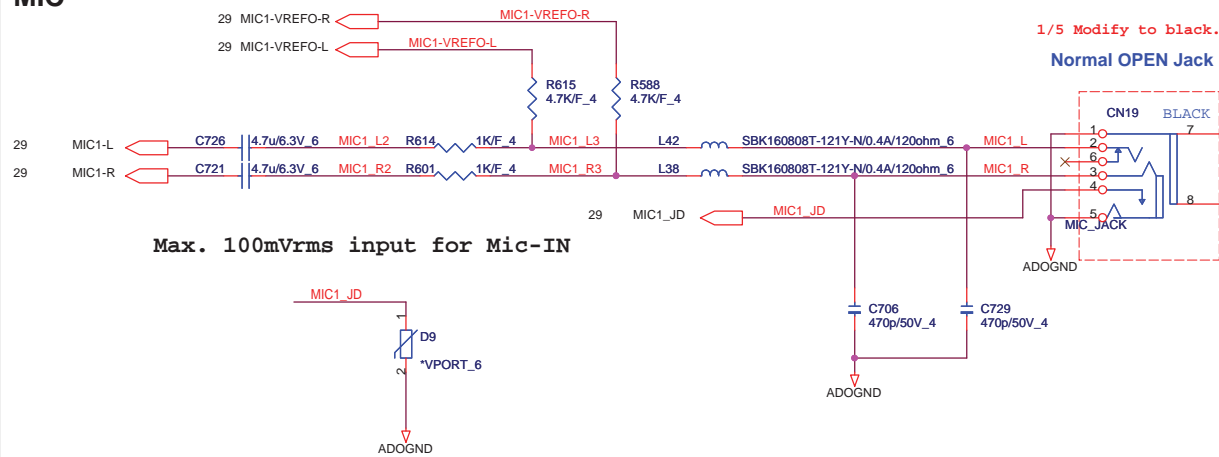
ODD POWER(ODD)



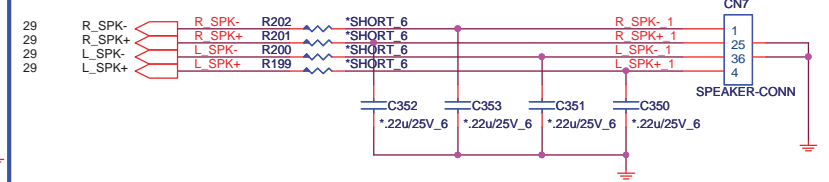
Quanta Computer Inc.
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Size	Document Number	Rev
	SATA-HDD/ODD/USB-ESATA	3B
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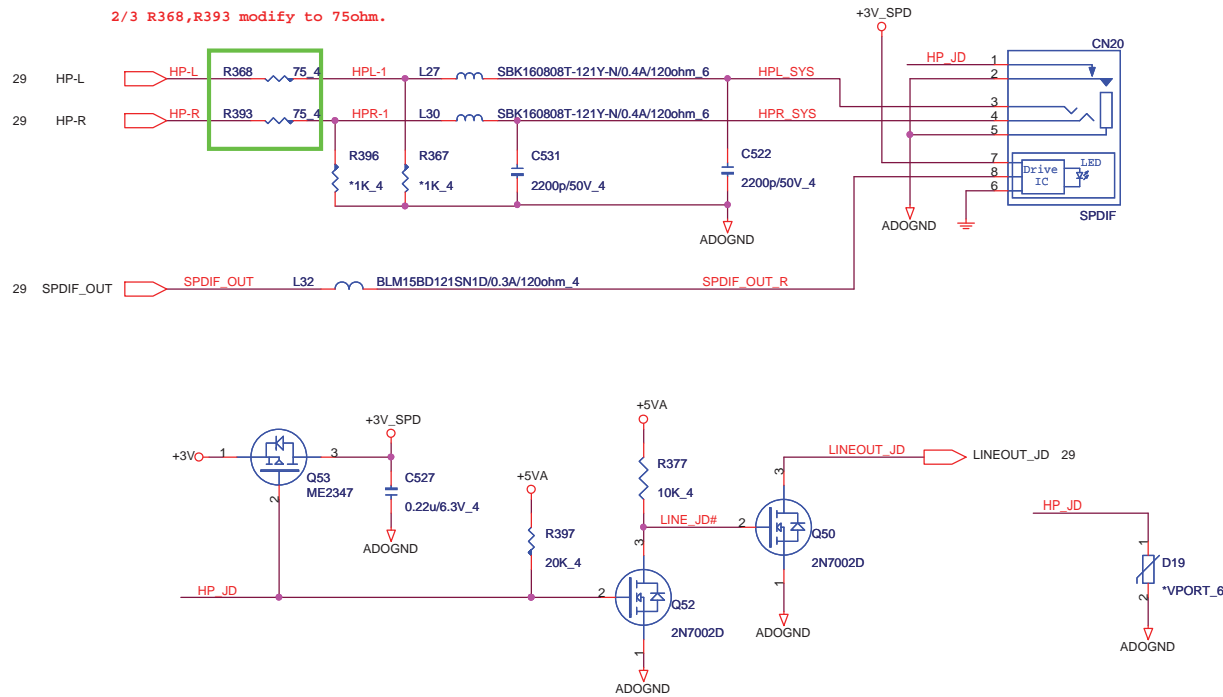



MIC

Internal Speaker

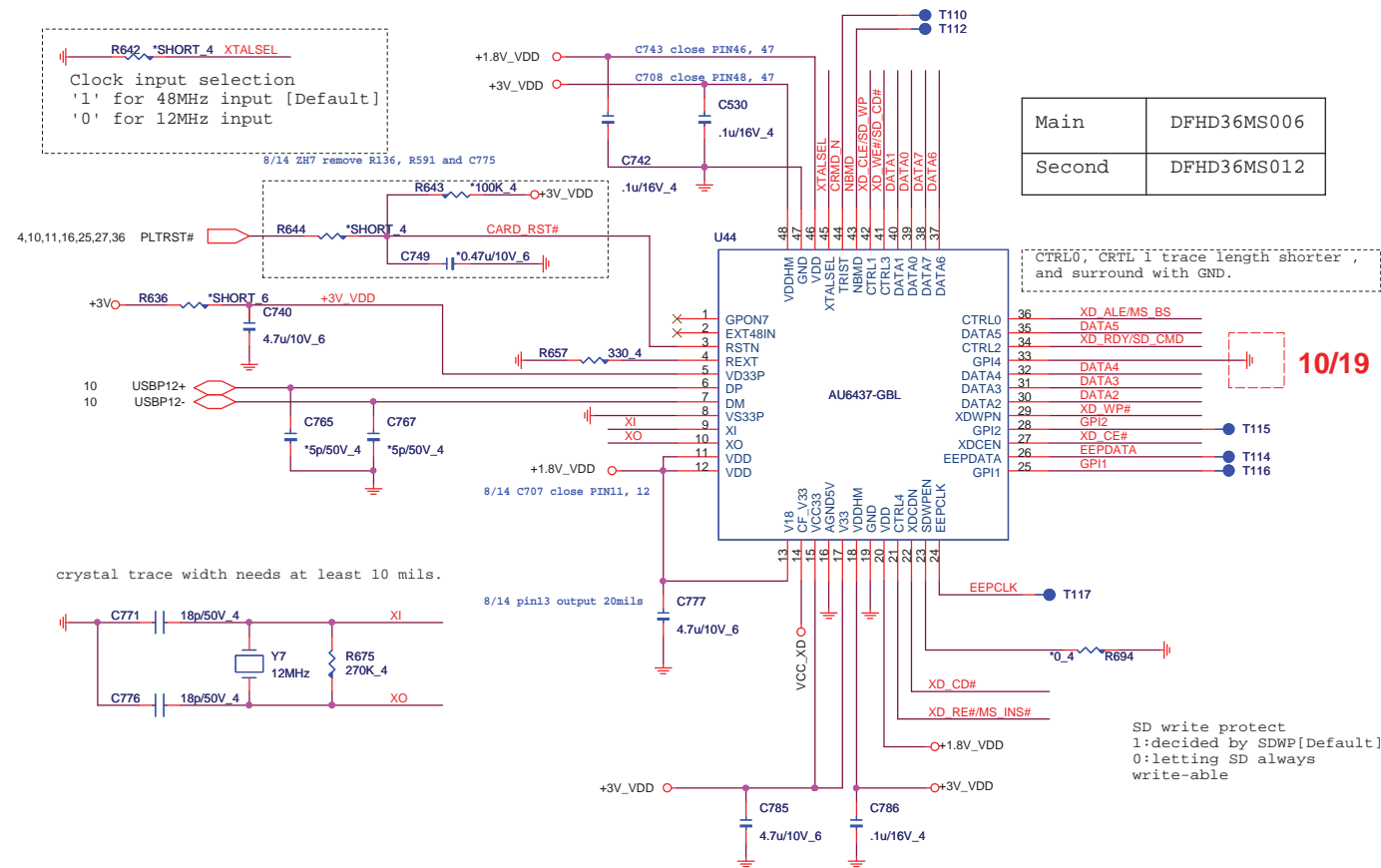


HP/SPDIF

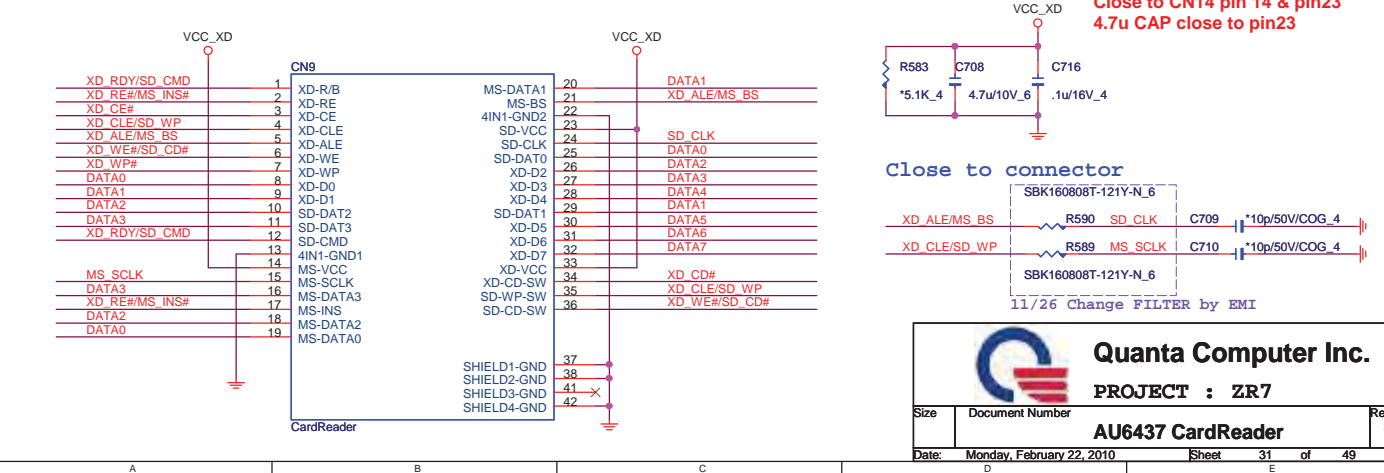


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Size	Document Number	Rev 3B
AMP /AUDIO JACK CONN		
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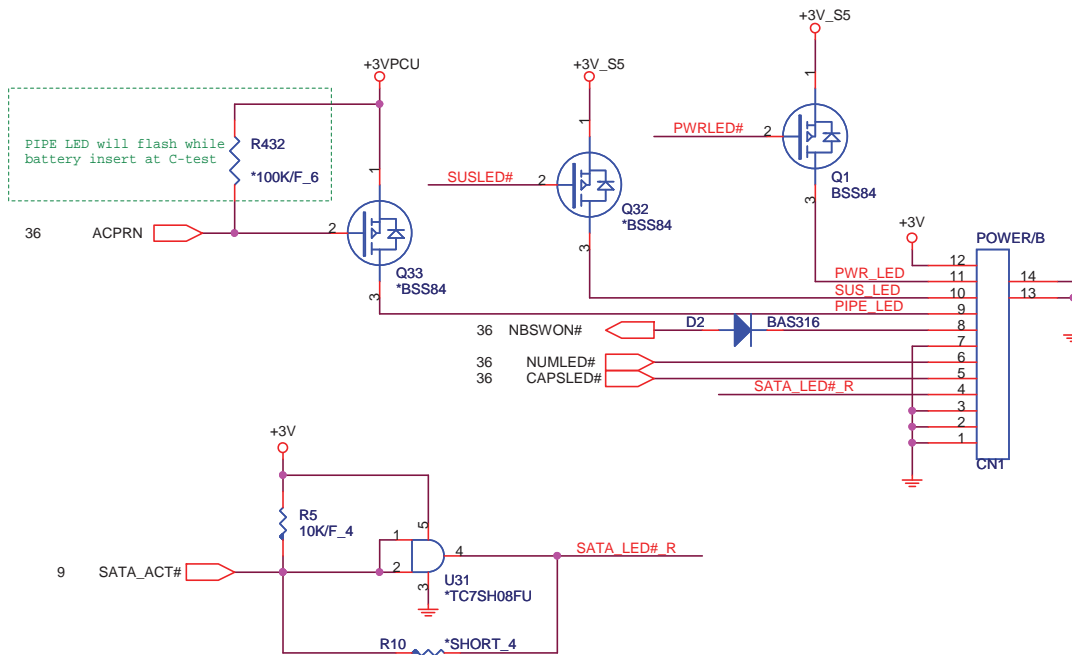
CARD READER Controller



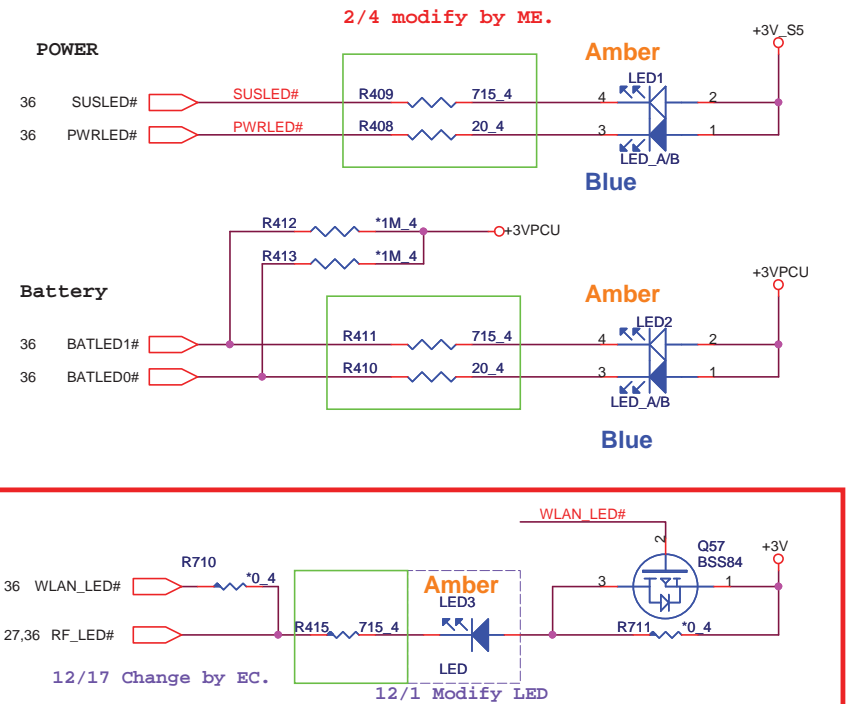
4 IN 1 CARD READER (MMC)



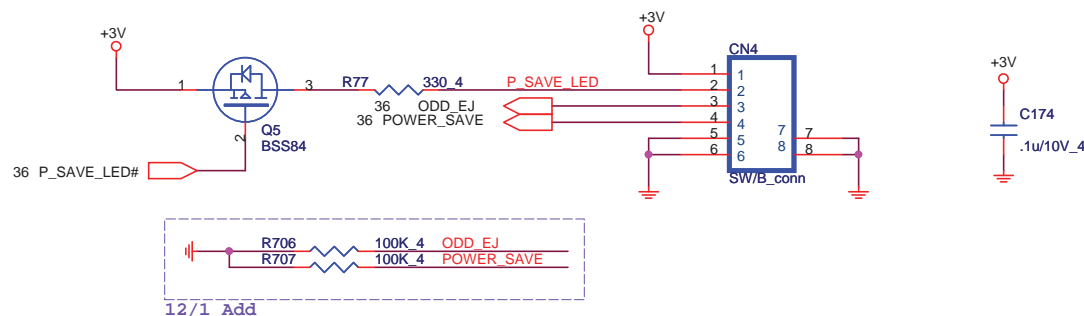
POWER BOARD CONN(UIF)




LED

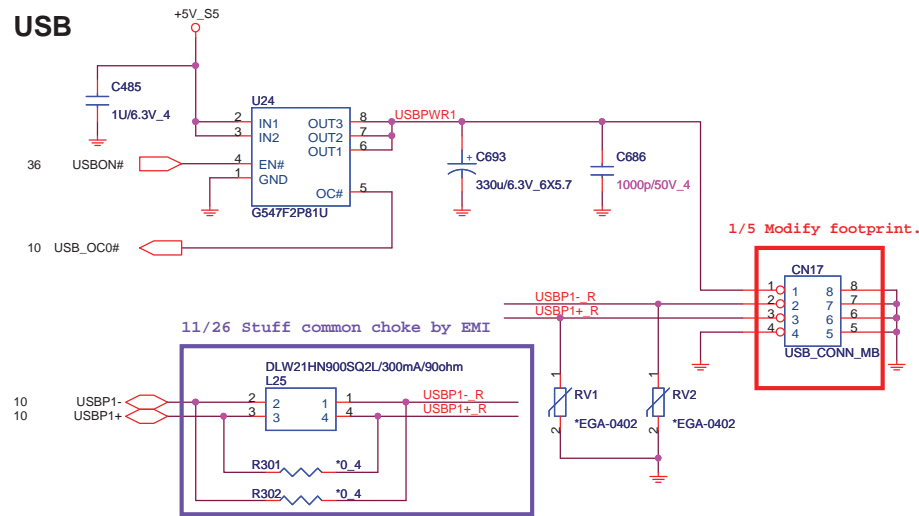


SW /B

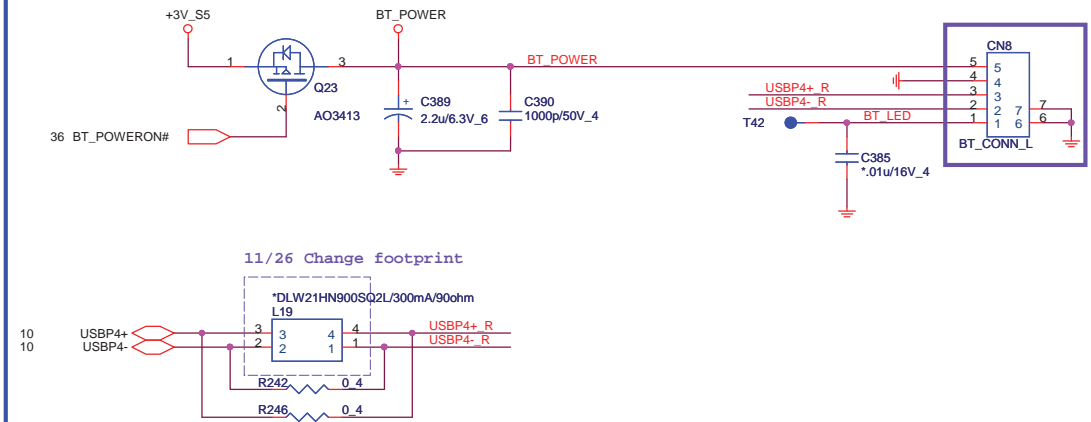


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		3B
Size	Document Number	
POWER/MMB/LAUNCH/LED		
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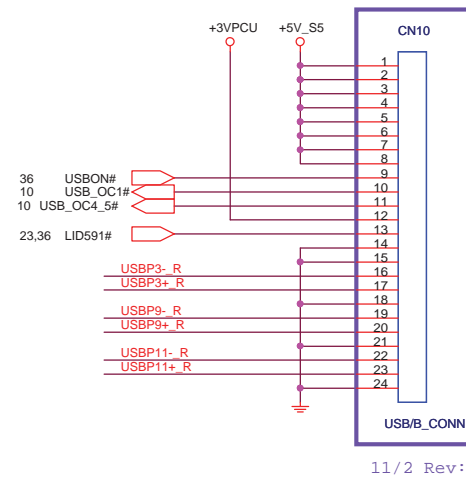
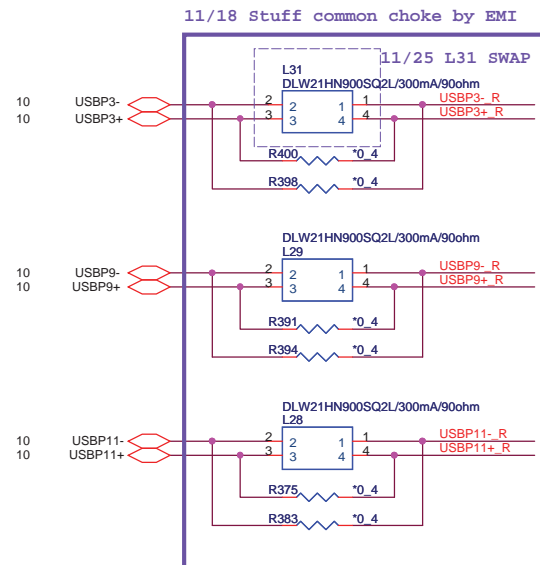
USB



BLUETOOTH CONNECTOR



USB/B



11/2 Rev:B Change CN10 P/N by PDC.



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USB/ BT

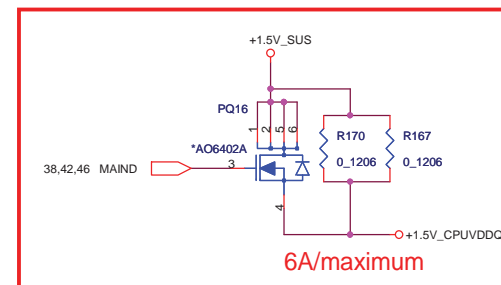
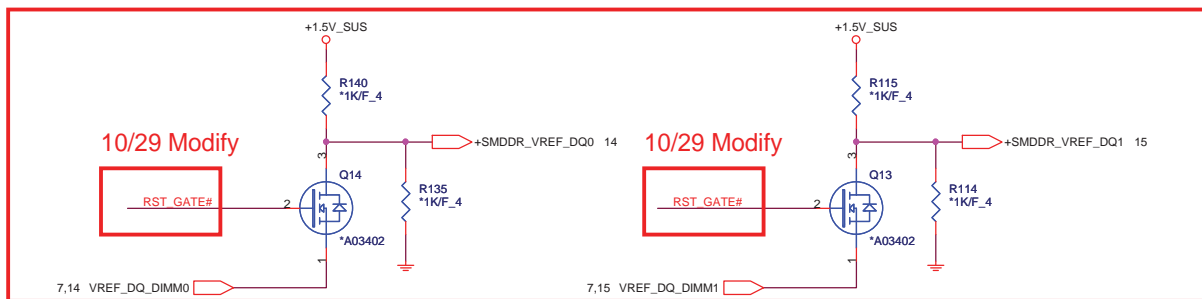
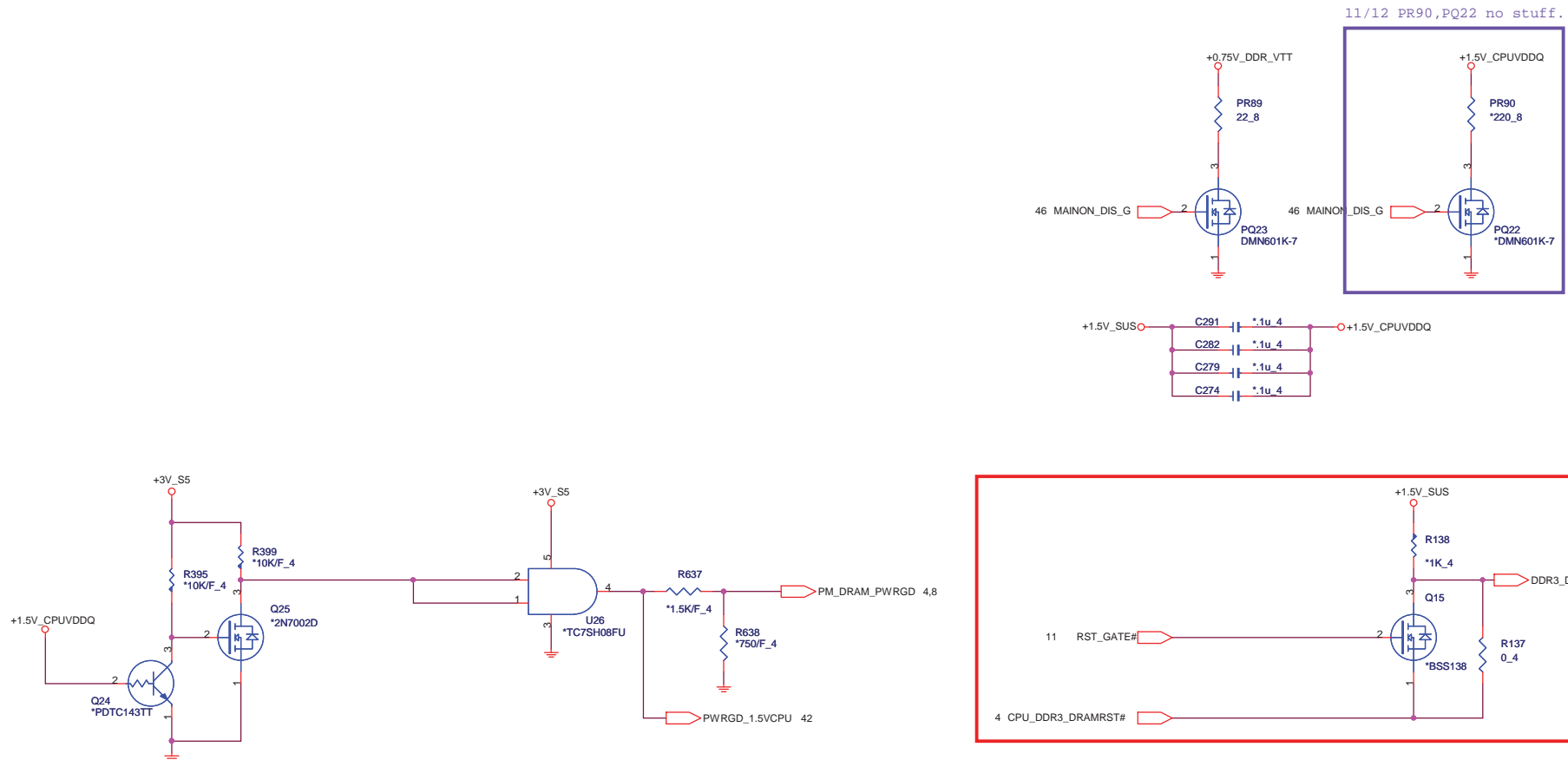
Rev
3B

Size	Document Number
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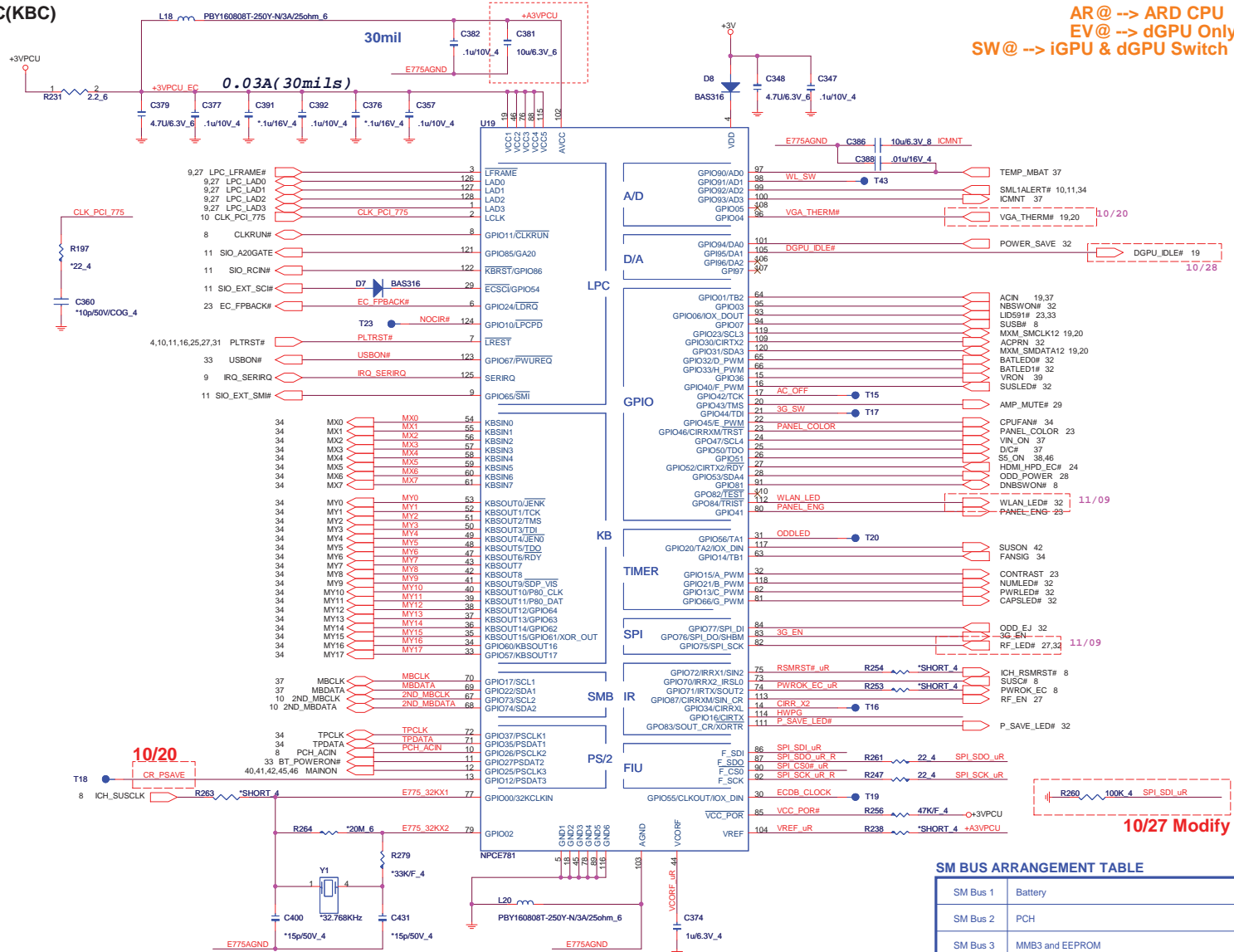
Date: Monday, February 22, 2010

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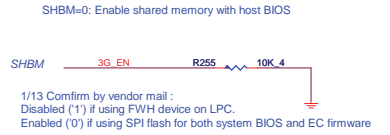




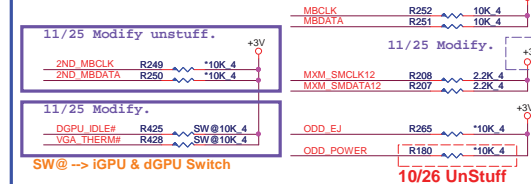
EC(KBC)



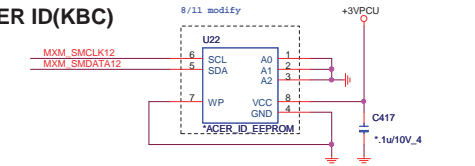
I/O ADDRESS SETTING(KBC)



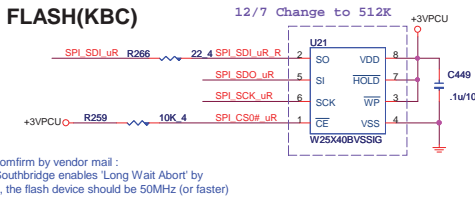
SM BUS PU(KBC)



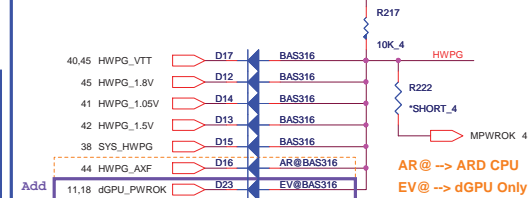
ACER ID(KBC)



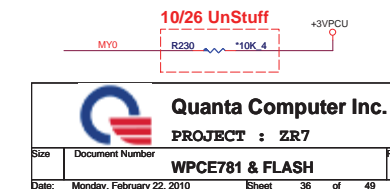
SPI FLASH(KBC)



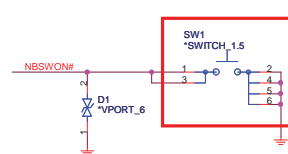
HWPG(KBC)



INTERNAL KEYBOARD STRIP SET(KBC)



POWER-ON Switch(KBC)



SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	MMB3 and EEPROM
SM Bus 4	HDMI Controller, MMB1, MMB2 and VGA Thermal

PR71, PR72, PR73, PR74, PR75, PR76, and PR77 deleted

100

6 H_VID1

6 H_VID4 

6 H_VID6

00433

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PC136

[illegible]

5/12 Change pr2

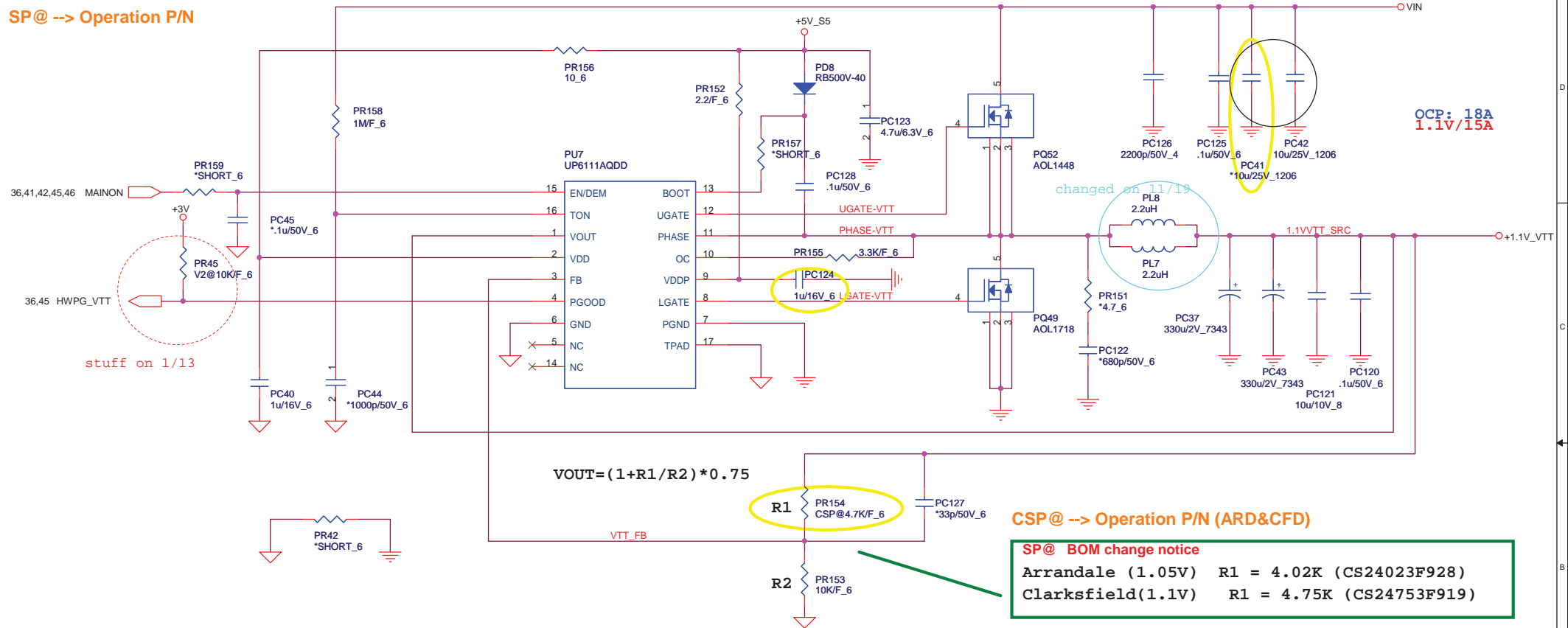
TABLE 1

PR63

SSSENSE PR71 *SHORT_4

[PWM]

SP@ --> Operation P/N



$$T_{ON} = 3.85p * R_{TON} * V_{out} / (V_{in} - 0.5)$$

$$Frequency = V_{out} / (V_{in} * T_{ON})$$

$$T_{ON} = 3.85p * 1m * 1 / (V_{in} - 0.5)$$

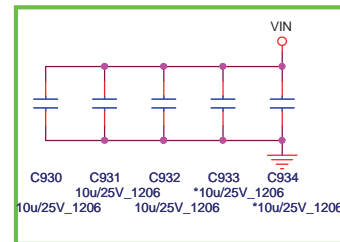
$$Frequency = 1 / (0.0036767) = 272K$$

AO1718 $R_{dson} = 3 \sim 4.3m\Omega$


$$I(\text{ripple current}) = (19 - 1.05) * 1.05 / (1u * 272k * 19) \sim 3.64A$$

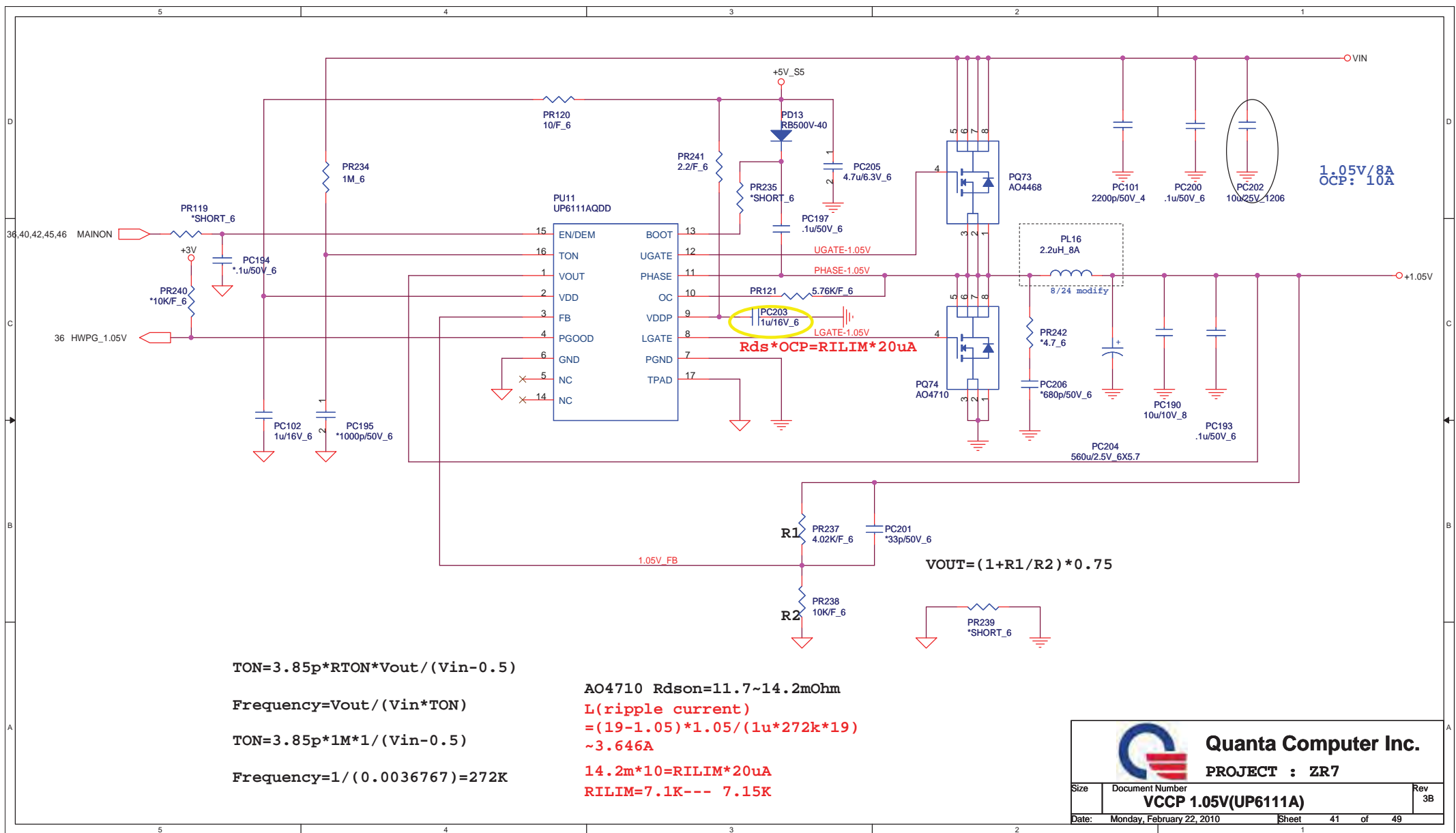
$$4.3m * 18 = R_{ILIM} * 20uA$$

$$R_{ILIM} = 3.87K \text{ --- } 3.92K$$

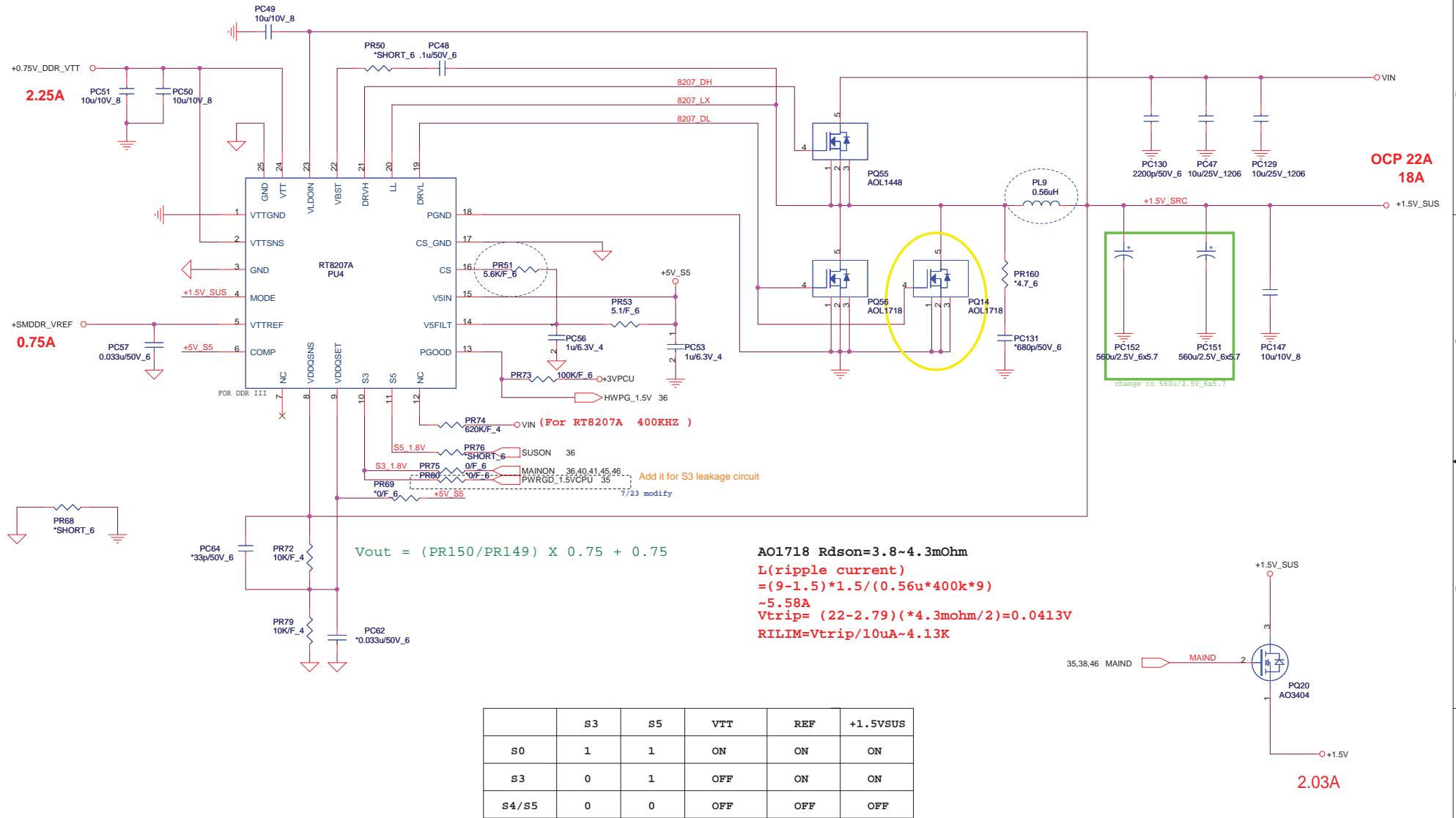


2/11 Add C930-C934 by monitor test.

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			+VTT (UP6111A)	3B
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[PWM]



11/16 Change VGPU_CORE to two phase solution.

SW@ --> iGPU & dGPU Switch

SW@ --> iGPU & dGPU Switch

11,47 dGPU_VRON

EV@ --> dGPU only

1/13 Add PR3032.

45,47 VGA_PG

19,47 GPU_VID1

11M@ --> N11M-GE1 Setitng

A horizontal number line with arrows at both ends. There are two tick marks. The tick mark on the right is labeled with the number 2. Above the tick mark at 2 is a blue closed circle. Above the tick mark to the left of 2 is a blue open circle. A blue line segment connects the open circle to the closed circle.

```
ripple current~3.2A--> current
limit=60mV(Vcc) & Rdcr_eq=2.69mohm
-->OCP=(60mV/2.69m+3.2A/2)*2=48A
```


TDC 36A/OCP 48A

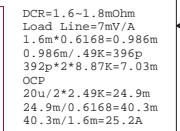
[illegible]

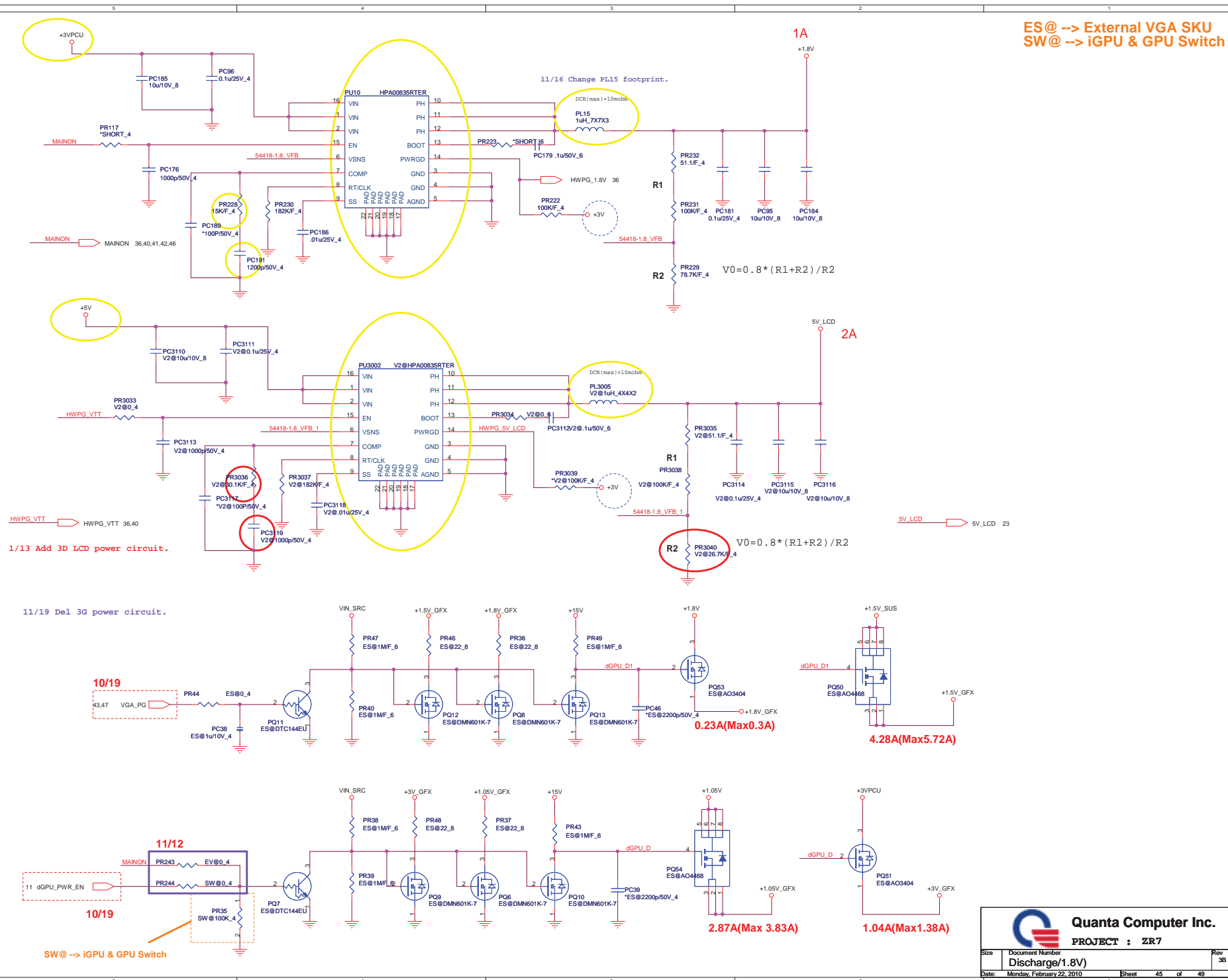
VID1

VID2

GPU_VID1	GPU_VID2	+VGPU_CORE
0	0	1.035V
1	0	0.95V
0	1	0.85V
1	1	0.8V

 Quanta Computer Inc. PROJECT : ZR7		
Size	Document Number GPU CORE(MAX17007)	Rev 3B
Date:	Monday, February 22, 2010	Sheet 43 of 49

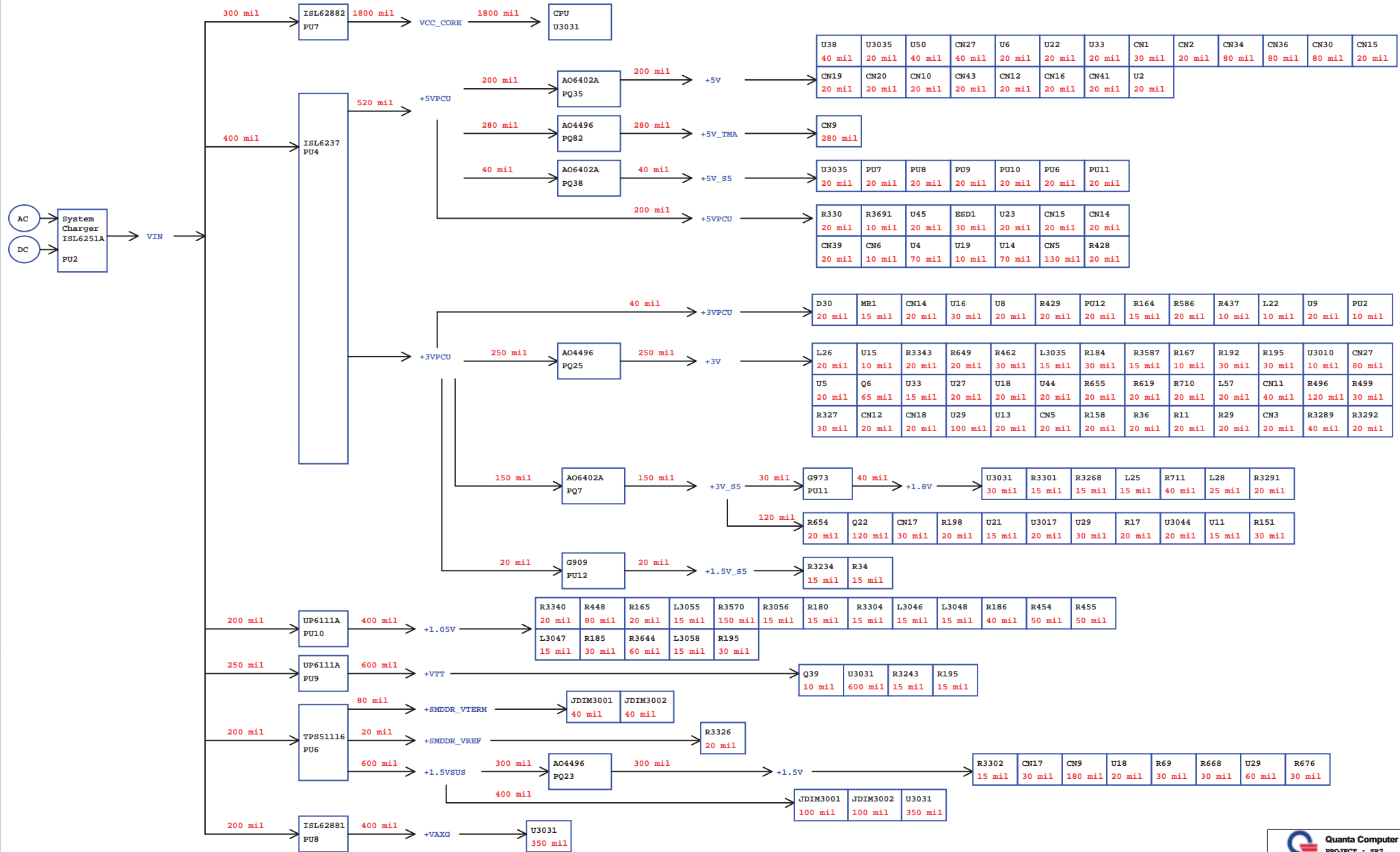




11P@ --> N11P-GE1 Setitng



Size	Document Number GPU CORE(MAX8792)	Rev 3B
Date:	Monday, February 22, 2010	Sheet 47 of 49



Model		REV	CHANGE LIST	ZXR7	
				FROM	To
ZXR7 MB			11/2 Page33 Change CN10 P/N by PDC.	1A	2A
			11/5 Page9 change R338 and R594 to 10K ohm by checklist.	1A	2A
			11/5 Page10 Add R699 connect XTAL25_IN to Gnd on EV sku and stuff Xtal components by checklist.	1A	2A
			11/5 Page12 un-stuff R318 and del C499 and add R698 connect VCCLAN to GND by checklist.	1A	2A
			11/9 Page32 change W/L LED signal to control by EC.	1A	2A
			11/9 Page16 Add EC pinR2112 for W/L LED control by EC.	1A	2A
			11/12 Page35 PR90,PQ22 no stuff.	1A	2A
			11/12 Page45 Add PR243,PR244 for option.	1A	2A
			11/16 Page23 CNI5 Add LVDS signal to two channel and change CN3 to Spin conn.	1A	2A
			11/16 Page43 GPU VCOORE power change to two phase solution.	1A	2A
2A			11/16 Page27 Add CN12 Spin conn for Touch screen by ME.	1A	2A
			11/16 Page44 Change P06 footprint by SMT.	1A	2A
			11/16 Page45 Change PL15 footprint to CHOKER-PCMC6437-3838W-WM4 by SMT.	1A	2A
			11/16 Page39 Change P08 footprint to qfn40-5x5-4-41p-0.75h-smt by SMT.	1A	2A
			11/16 Page37 Change P03 footprint to QFN28-SX5-5-33P-SMT by SMT.	1A	2A
			11/18 Page10 Delete R597, C444,C445 for cancel 3G function.	1A	2A
			11/18 Page30 R368,R393 modify from 47ohm to 56ohm by Realtek.	1A	2A
			11/18 Page10 Change BOARD_ID0-2 to BOARD_ID1-3.	1A	2A
			11/18 Page11 Change GP707 to ROM0_ID0 and reserve R439 PD.	1A	2A
			11/18 Page36 Add D23 to connect to dGPU_PWRON on EV sku.	1A	2A
3A			11/18 Page9 Change P/N follow ZXR7B that use right angle connector.	1A	2A
			11/18 Page27 Reserve C919, CN22 for MV IR signals on B-test.	1A	2A
			11/19 Page3 Change U39 PH to AL00197002 by vendor.	1A	2A
			11/19 Page31 Change CN9 footprint & P/N follow ZXR7B.	1A	2A
			11/19 Page27 Add R697 for MI-FI.	1A	2A
			11/19 Page11 Add R442, R440 to dGPU_PWRON_B and stuff R322 on EV sku.	1A	2A
			11/19 Page23 Modify CN5 pin define.	1A	2A
			11/20 Page43 Add PR124 on EV sku.	1A	2A
			11/20 Page12-14 Change core logic cap .1uF CH41003B35 to CH4102K1B03 by SMT.	1A	2A
			11/20 Page45 del 3G power circuit.	1A	2A
3B			11/20 Page34 del HOLE10,Add HOLE5,HOLE6,HOLE7,HOLE8,HOLE11,HOLE12,HOLE14,HOLE15,HOLE17,HOLE18,HOLE20,HOLE24,HOLE25,HOLE26,HOLE30 P/N	1A	2A
			11/25 Page10 Q26,Q29 change to unstuff , Add R700,R701 0 ohm for S3 leakage	1A	2A
			11/25 Page20 C111 change to CC7341 package	1A	2A
			11/25 Page34 Change HOLE5,HOLE12 footprint to H-C236D142P2 , Change HOLE5,HOLE7,HOLE11 footprint to H-TC197D122P2 ,	1A	2A
			Change HOLE14,HOLE15,HOLE17,HOLE18 footprint to H-TC236D142P2 , Change HOLE20,HOLE24,HOLE26 footprint to H-TC236D142P2 , Change HOLE8 footprint to O-ZR7-1-B	1A	2A
			11/25 Page36 R425 change to dGPU_IDLE# signal and value to SW SKU , R428 change value to SW SKU , R249,R250 change to unstuff	1A	2A
			11/25 Page28 Add C920,C921,C923,C924 0.1uF for EMI	1A	2A
			11/25 Page33 L31 BMAP for Layout House	1A	2A
			11/25 Page27 Modify L3B7B8_7738 net name to PL3B7B8	1A	2A
			11/26 Page33 Change L19,L25 footprint , Stuff L25 common choke & unstuff R301,R302 by EMI	1A	2A
2A			11/26 Page21 Change L2 footprint	1A	2A
			11/26 Page23 Change R589,R590 to PLITER for EMI	1A	2A
			11/26 Page28 Add C925,C926,C927 for EMI	1A	2A
			11/26 Page11 Modify R422 Value to IVB SKU	1A	2A
			11/27 Page11 Del R440	1A	2A
			11/27 Page20 CNI1,C105 change CC0603 package	1A	2A
			11/27 Page16 C94,C109 change CC0603 package	1A	2A
			11/27 Page23 Add CNI5 pins4 to GND	1A	2A
			11/27 Page27 Add L46,L47,R702,R703,R704,R705 by EMI	1A	2A
			11/27 Page10 Modify C699,C703 to 27pF	1A	2A
3A			11/27 Page18 Modify C601,C600 to 27pF	1A	2A
			12/1 Page27 Modify CN12 to 6 pin connector	1A	2A
			12/1 Page32 Modify LED3 & Add R706,R707 PD by EC OED_EJ & POWER_SAVE	1A	2A
			12/1 Page9 Add R708,R709 by EPI ROM	1A	2A
			12/18 Page32 Add R710,R711,Q57 by EC.	2A	3A
			12/18 Page23 Add R712,R713 by 3D features.	2A	3A
			12/18 Page47 Change P26 footprint to choke-mp1136-2r2-smt by SMT.	2A	3A
			12/29 Page27 Change CN21 footprint to MIPCI-80005FW05200pl-52P-smt by SMT.	2A	3A
			12/29 Page23 Add P1 by safety.	2A	3A
			12/29 Page24 Change Q16, Q45 P/N & add P2 by RMDI submit and safety; del U15, U16, U18.	2A	3A
3B			12/29 Page30 Change CN19 color to black P/N: DFTJ08P130 by ACER.	2A	3A
			1/5 Page33 Change CN17 footprint to USB-UB1110C-BASED-7P-4P-R-V-SMT by PDC.	2A	3A
			1/7 Page23 Change Q12 of dGPU_selectcs signal design by leakage issue.	2A	3A
			1/7 Page9 Change EPI P/N to DFTD08P130 by ME issue.	2A	3A
			1/8 Page27 Change CN12,CN22 6pin conn footprint for Touch Screen and IR.	2A	3A
			1/11 Page23 Add L48 & stuff L2 and un-stuff R28 and R29 by EMI.	2A	3A
			1/11 Page24 Add C928 by EMI.	2A	3A
			1/13 Page12,36 Change C711,C382 to 10U 6.3V.	2A	3A
			1/14 Page23 Change LVDS connector Pin4 define from NC to LCDVCC & add J3 by 3D PWR.	2A	3A
			1/14 Page28 Change C218,C678 to 10U/10V_8 and footprint 0805.	2A	3A
2A			2/3 Page16-22 Change U33 footprint to fcbga733-vidia-nlp-es-a1 by NV.	2A	3A
			2/3 Page 30 Change R368,R393 to 75ohm.	3A	3B
			Power Modify	1A	2A
			11/19 Take out JP12, JP9, JP5, JP6, JPT, JP19, JP20, JP8, JP10, JP11,JP13, JP15, JP16, JP1, JP17, JP14, JP18.	1A	2A
			11/19 Page38 Change PC139 value; change PR114 from 181K to 181K, PR115 from 220K to 200K,PR106 from 100K to 1K,PR105 from 200K to 150K.	1A	2A
			11/19 Page39 Change R27,P68 from 1.0uR to 3.2uR.	1A	2A
			11/19 Page39 Change D06,PL11 from DC-3670W000 to CV-18V0M204.	1A	2A
			11/19 Page43 Reserve PC1030.	1A	2A
			11/23 Page37 PR19 change to 150K , PR20 change to 39K , PC112 change to 1U 25V	1A	2A
			12/29 Page47 Change PL7,P68,PL45,PL16 footprint to CHOKER-PCMC6437-3838W-SMT by SMT.	1A	2A
3A			12/29 Page37 Change PR136 footprint to RC3720-SMT by SMT.	2A	3A
			1/5 Page37-48 Change Footprint from CHOKER-ETQP4LR36WFC to CHOKER-ETQP4LR36WFC-SMT by PDC.	2A	3A
			1/11 Page37 Add PC3100-PC3109 by EMI.	2A	3A
			1/11 Page47 Change value of PQ7021,PL6,PL3004 by ROM.	2A	3A
			1/13 Page43 Reserve PR3032 by PWR.	2A	3A
			1/13 Page45 Reserve circuit of LCDVCC by PWR.	2A	3A
			2/10 Page37 Reserve ECI-RC3 by EMI.	3A	3B
			2/11 Page38 Del PD3 by power.	3A	3B
			2/11 Page40 Add C930-C934 by monitor test.	3A	3B
				3A	3B
3B					
Quanta Computer Inc.					
PROJECT : ZR7					
Change list2					
DQC NO.			PROJECT MODEL :	ZR7	APPROVED BY:
			PART NUMBER:		DRAWING BY:
			DATE:		2009/11/06
			REVISION:		1A